



P55H-AK

V : 1.0

(LGA1156P Processor with DDR3 SDRAM Mainboard)

SCHEMATICS TABLE:

| Page | Index |
|------|---------------------------|
| 1 | Cover Page |
| 2 | Block Diagram |
| 3 | LGA1156 CPU/GPU/PEG/DMI |
| 4 | LGA1156 DDR3 MEMORY |
| 5 | LGA1156 PWR/GND |
| 6 | DDR3 Channel0 DIMM1&DIMM2 |
| 7 | DDR3 Channel1 DIMM3&DIMM4 |
| 8 | CLK |
| 9 | CPU VCORE UP6225 |
| 10 | CPU VTT |
| 11 | DC-DC |
| 12 | Front Panel,FAN,PowerConn |
| 13 | nVidia NF200 - 1 |
| 14 | nVidia NF200 - 2 |
| 15 | PCH PCI/USB/SATA/PCIE/DMI |
| 16 | PCH CLK/GPIO/DISPLAY |
| 17 | PCH PWR/GND |

| Page | Index |
|------|----------------------|
| 18 | PLX PEX8608 |
| 19 | PCIE1X SLOT |
| 20 | USB/SPI/Rear IO |
| 21 | PCI SLOT |
| 22 | LPC SIO-ITE8721 |
| 23 | EUP, PS/USB |
| 24 | AUDIO ALC889 (CHIP) |
| 25 | AUDIO ALC889 (CONN) |
| 26 | PCIE LAN RTL8111E #1 |
| 27 | PCIE LAN RTL8111E #2 |
| 28 | SATA3.0 |
| 29 | E-SATA3.0 |
| 30 | USB3.0 (CONNECTOR) |
| 31 | USB3.0 (HEADER) |
| 32 | PCIEX16 Slot1 |
| 33 | PCIEX16 Slot2 |
| 34 | PCIEX16 Slot3 |
| 35 | VCORE MOS |

REVISION HISTORY:

| Rev | Date | Notes |
|-----|-------|---|
| A | 04/21 | Initial official release |
| B | 04/23 | Modify BR04 : Connect DP_REF_CLK to CLK GEN and BR04 its STRAP Modify BOM : Remove EEPROM of PX8608 |
| B | 04/27 | Modify CLK : Connect PEX8608 CLK to CLK GEN Connect PCIE 1X slot CLK to PCH Modify VDIMM PWM compensation |
| B | 04/30 | PCH add FHW header for BIOS flash Fixed Mini-Dim library error |
| B | 05/03 | Modify Deep Green Circuit |
| B | 05/05 | USB DUAL PWR EN (USBPWR_EN) |
| B | 05/11 | F_USB3.0 -> USB2 signal connect to PCH |
| B | 05/13 | Add Audio ESD Resister Connect BR04 temp sense to IO |
| B | 05/17 | Fix P29. 88SE9128 pin57 net issue |
| B | 05/18 | Modify USB3.0_LAN connector pcb footprint for UDE |
| B | 05/20 | Modify ESD Components Modify VCORE Compensation Modify CPU VTT Compensation |
| B | 05/21 | Modify VCORE Value For Transient |
| B | 05/24 | Modify PWR-MOS, PWR-CHOKE PCB footprint |
| B | 05/25 | Fixed PEX16-3 present issue |
| B | 05/28 | SW VDD1.2 modify to VDD1.5 V_1P05_PCH source changed from VDD1.2 to VDD1.5 VDD1.2 changed to linear from VDD1.5 |
| 1.0 | 06/24 | Modify compensation of VCORE PWM to fix Lynnfield CPU reliability(BOM) Modify RT8108 value to solve LDO MOS thermal issue(BOM) Fix PWR BTN no function issue Upgrade Deep-Green circuit design |

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

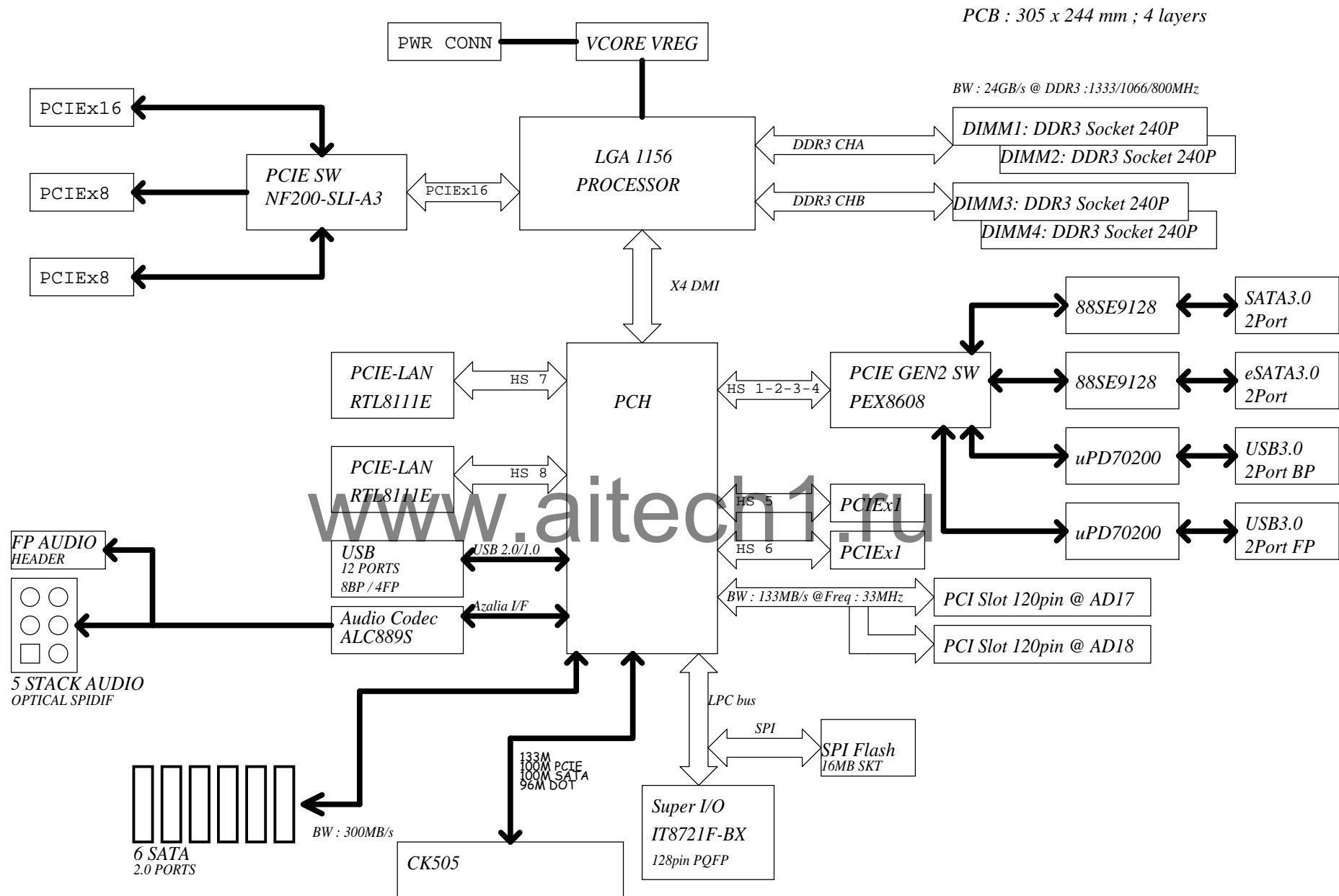
DESIGN NOTE: Example text for the design note to show the note inside the colored box.

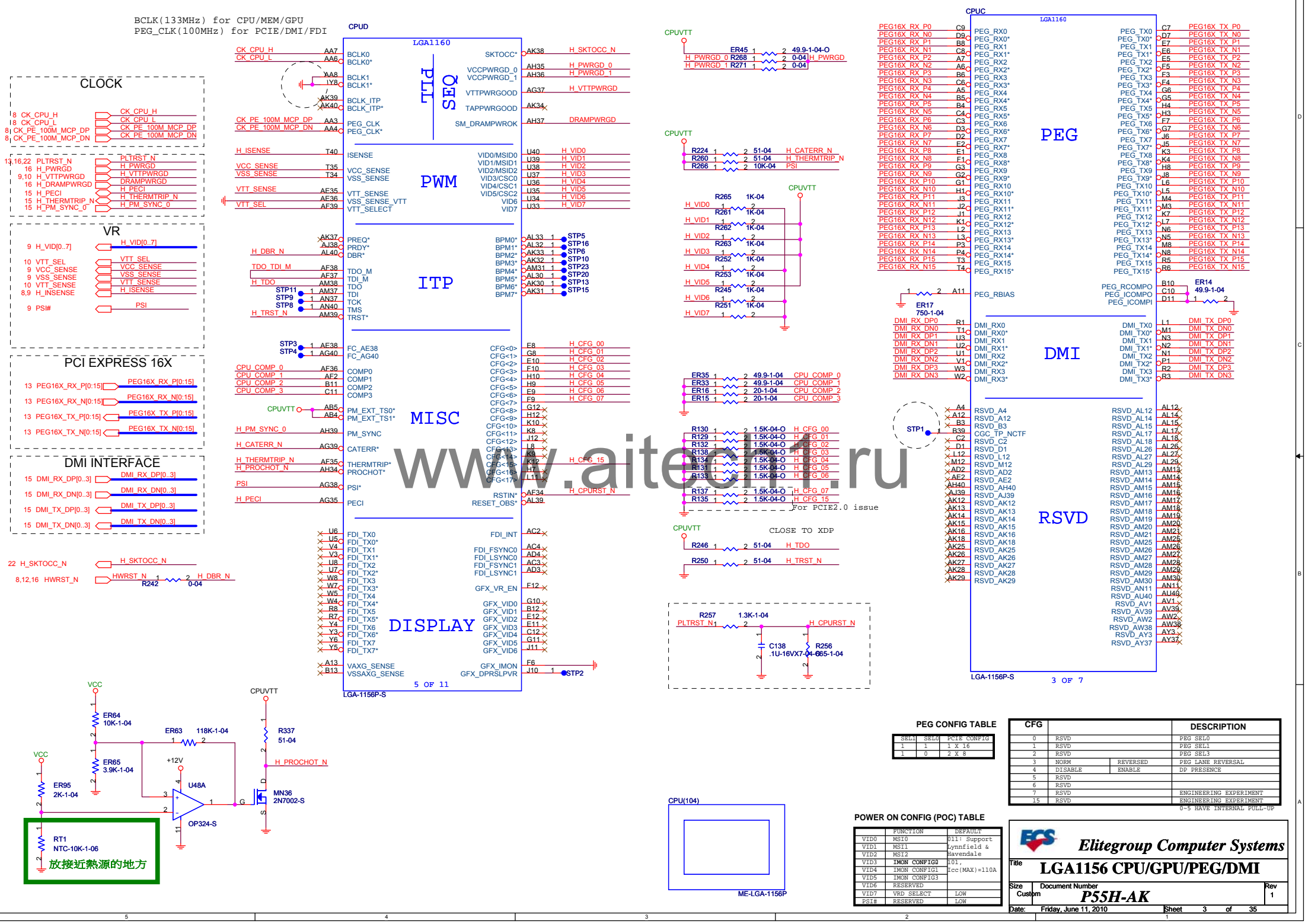
2) DESIGN NOTES in yellow are notes of caution.



3) DESIGN NOTES in red are critical, and must be understood and followed.

| | | |
|-----------------------------|--------------------------------|--------------|
| Elitegroup Computer Systems | | |
| Title Cover Page | | |
| Size Custom | Document Number P55H-AK | Rev 1 |
| Date: Friday, June 25, 2010 | Sheet 1 | of 35 |




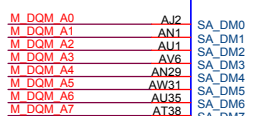
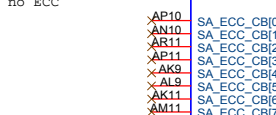
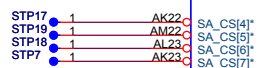
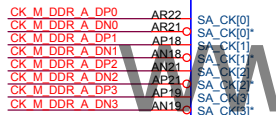
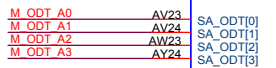
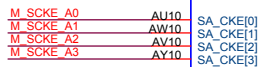
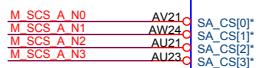
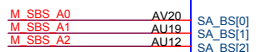
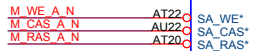
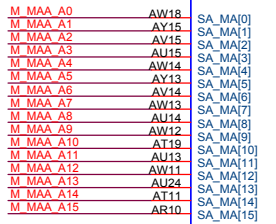
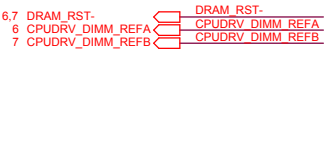
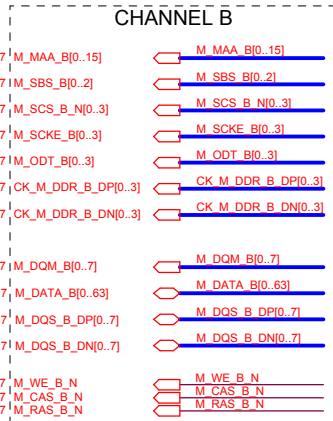
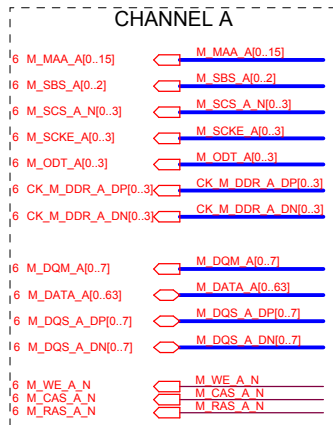


| SEL1 | SEL0 | PCIE CONFIG |
|------|------|-------------|
| 1 | 1 | 1 X 16 |
| 1 | 0 | 2 X 8 |

| CFG | | | DESCRIPTION |
|-----|---------|----------|------------------------|
| 0 | RSVD | | PEG SEL0 |
| 1 | RSVD | | PEG SEL1 |
| 2 | RSVD | | PEG SEL3 |
| 3 | NORM | REVERSED | PEG LANE REVERSAL |
| 4 | DISABLE | ENABLE | DP PRESENCE |
| 5 | RSVD | | |
| 6 | RSVD | | |
| 7 | RSVD | | ENGINEERING EXPERIMENT |
| 15 | RSVD | | ENGINEERING EXPERIMENT |

| | FUNCTION | DEFAULT |
|------|--------------|-----------------|
| VID0 | MSIO | 011: Support |
| VID1 | MSI1 | Lynnfield & |
| VID2 | MSI2 | Havendale |
| VID3 | IMON CONFIG0 | 101, |
| VID4 | IMON CONFIG1 | Icc (MAX) = 110 |
| VID5 | IMON CONFIG3 | |
| VID6 | RESERVED | |
| VID7 | VRD SELECT | LOW |
| PSI# | RESERVED | LOW |

| | | | |
|---|--|------------------------------------|-----------------|
|  | | Elitegroup Computer Systems | |
| Title LGA1156 CPU/GPU/PEG/DMI | | | |
| Size Custom | Document Number P55H-AK | | Rev 1 |
| Date: Friday, June 11, 2010 | Sheet 3 | of 35 | |



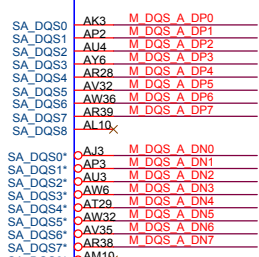
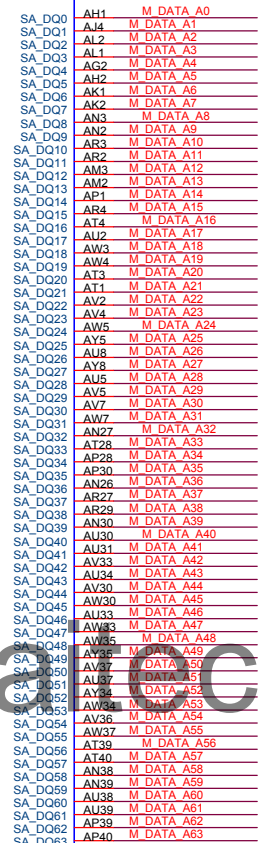
W/S=6/10

CPUA

LGA1160

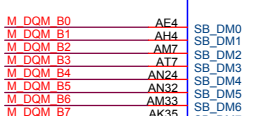
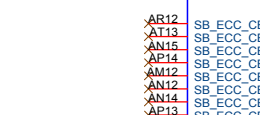
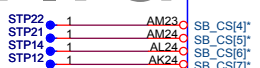
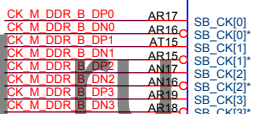
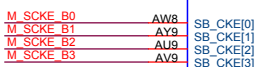
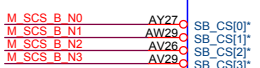
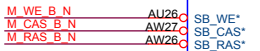
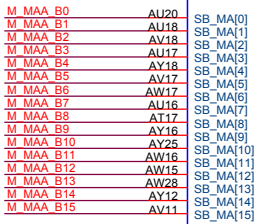
LGA-1156P-S

1 OF 7



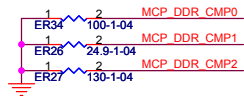
CPUB

LGA1160



LGA-1156P-S

DDR_B

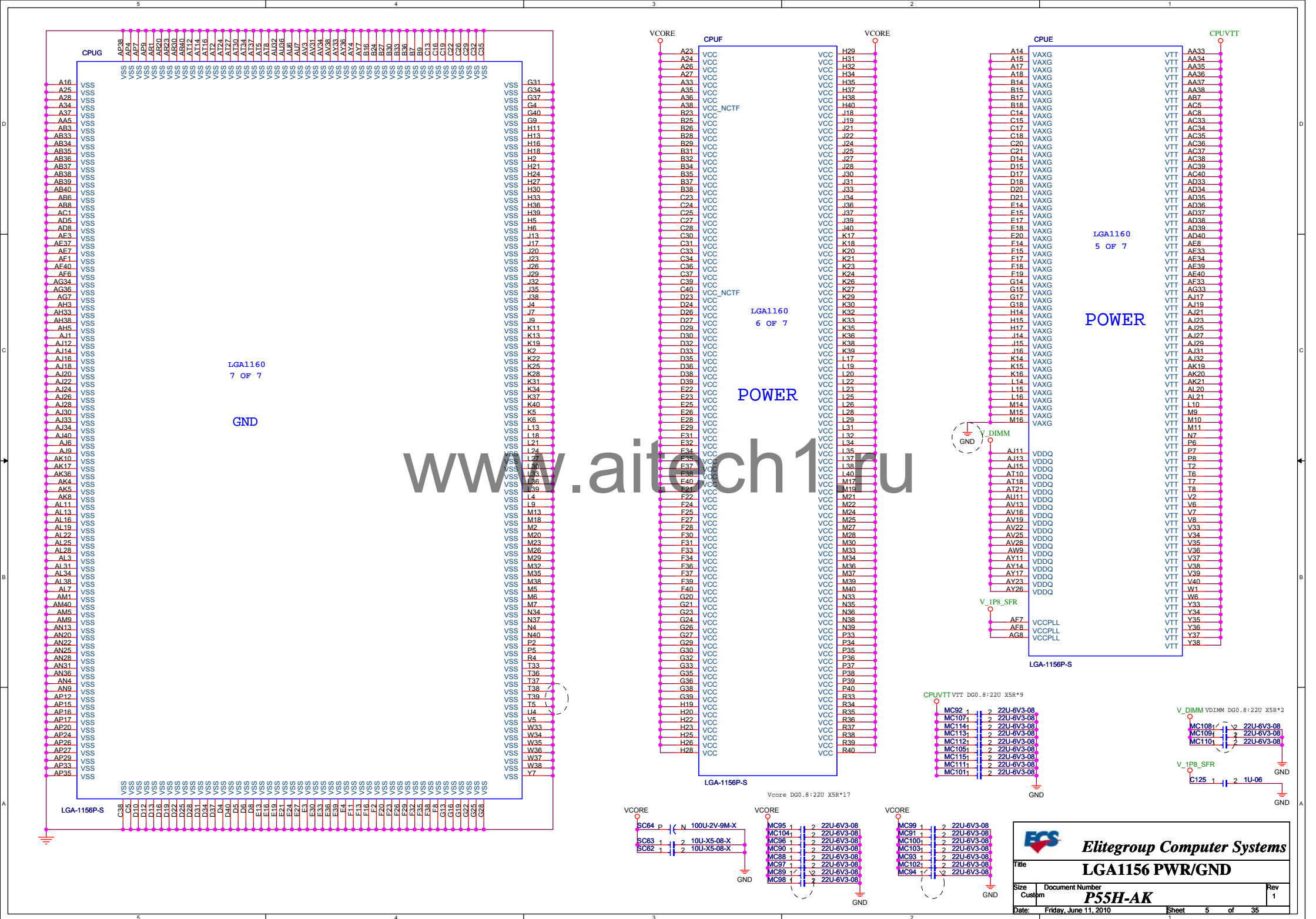


Elitegroup Computer Systems

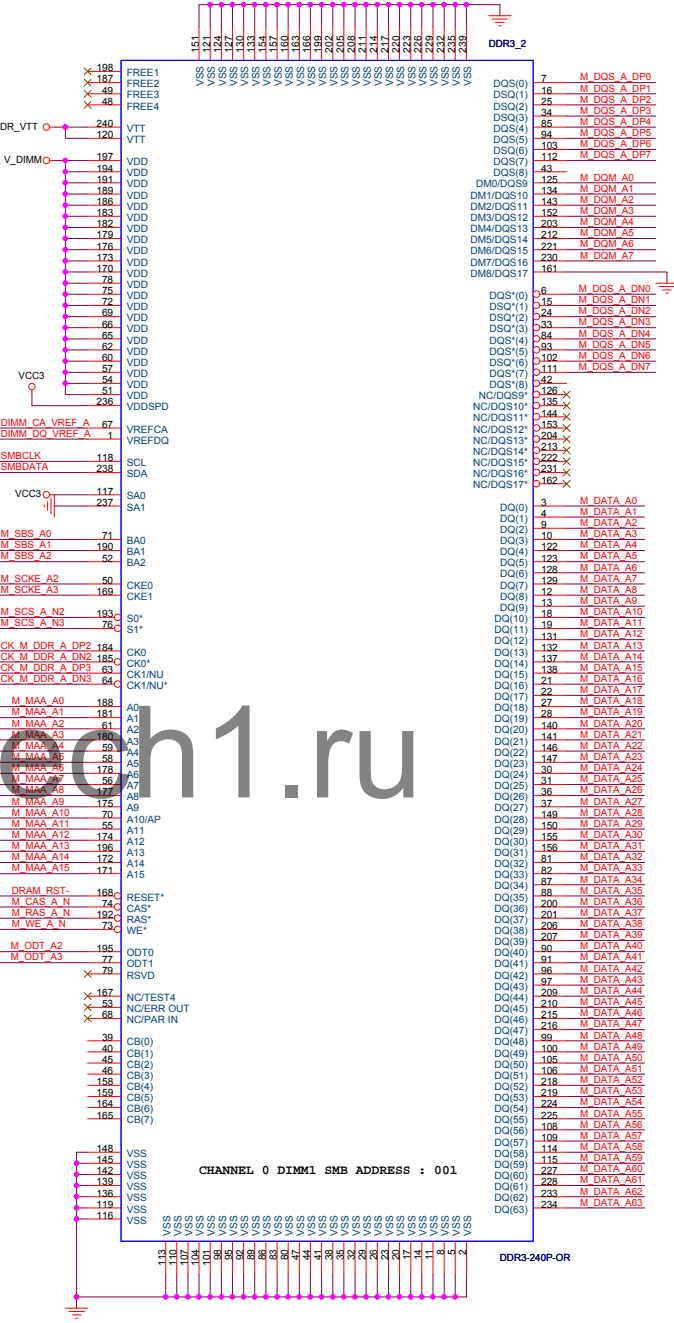
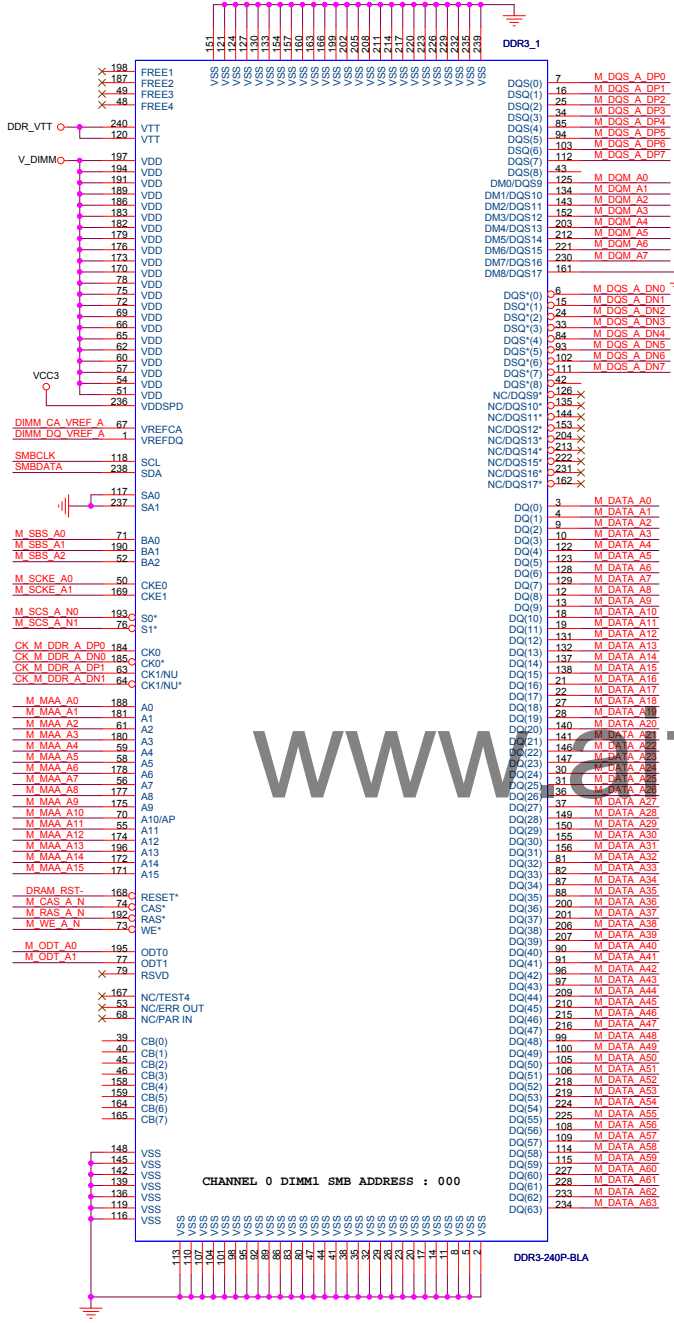
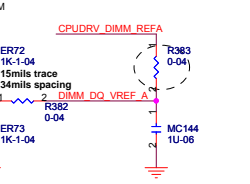
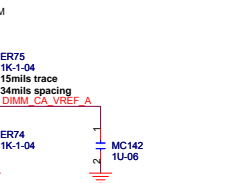
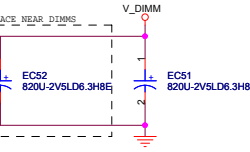
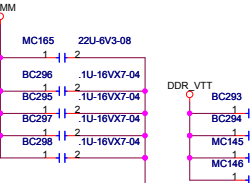
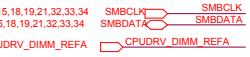
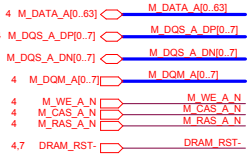
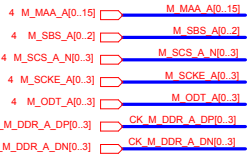
Title LGA1156 DDR3 MEMORY

Size Document Number P55H-AK Rev 1

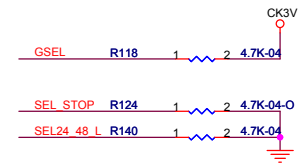
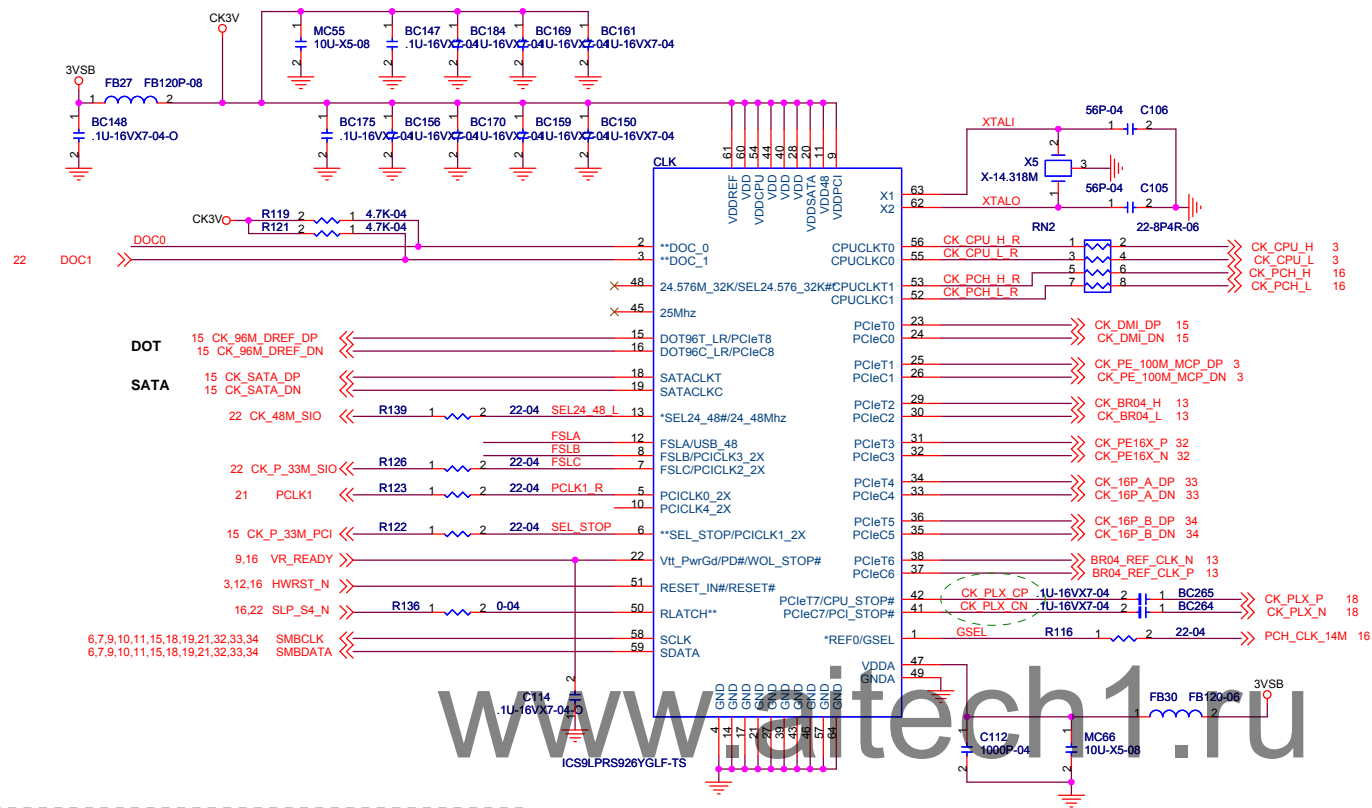
Date: Friday, June 11, 2010 Sheet 4 of 35



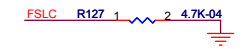
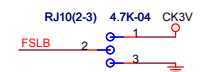
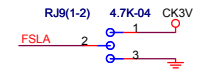
ChannelA



[illegible]



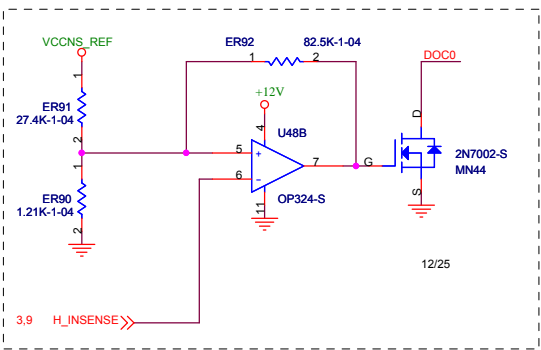
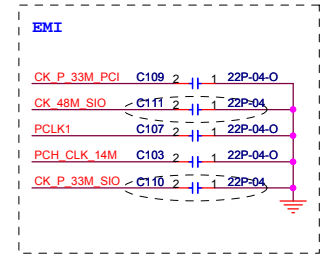
| | 1 | 0 |
|--------------|--------------|---------|
| SEL_STOP | CPU/PCI_STOP | PCIeCLK |
| GSEL | 96M | 100M |
| SEL24_48# | 24M | 48M |
| SEL24_5_32K# | 24.576M | 32KHz |



FSLB,FSLA = 01, CPU_CLK = 133MHz

| Bit1 | Bit0 | CPU CLOCK (MHZ) |
|------|------|-----------------|
| 0 | 0 | 266.66 |
| 0 | 1 | 133.33 |
| 1 | 0 | 200.00 |
| 1 | 1 | 166.66 |

| CK3V | 3VSB | VCC3 |
|----------|------|------|
| RLATCH** | V | X |
| resister | | |



External Connection

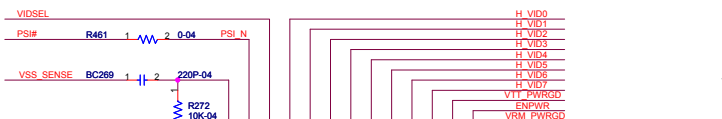
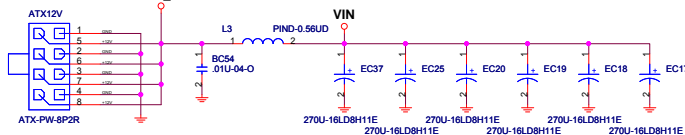
VCC
VCCORE
CPUVTT
SMBCLK
SMBDATA

3 H_VID[0..7] >> H_VID[0..7]
3 VCC_SENSE >> VCC_SENSE
3 VSS_SENSE >> VSS_SENSE
3.10 H_VTTPWRGD >> VTT_PWRGD
8.16 VR_READY << VRM_PWRGD
10 LVCORE << VCCORE_FB
3 PS# << PS#
3.8 H_INSENSE << H_INSENSE
35 UG1[1:12] << UG1[1:12]
35 PHASE1[1:12] << PHASE1[1:12]
35 LG1[1:12] << LG1[1:12]
35 SENSE[1:12] << SENSE[1:12]
35 IS_1[1:12] << IS_1[1:12]
35 OUT1_2 << OUT1_2
35 OUT3_4 << OUT3_4
35 OUT5_6 << OUT5_6
35 OUT7_8 << OUT7_8
35 OUT9_10 << OUT9_10
35 OUT11_12 << OUT11_12
22 CPULED_EN << CPULED_EN

BC276 1 2 68P-04
R299 1 2 20K-1-04
BC275 1 2 010U-04
R270 1 2 22-1-04
BC288 2200P-04
R275 1 2 1.5K-1-04
VCC_SENSE
R330 82K-1-04
R329 100K-04-0
SENSE7
OUT1_2
SENSE8
R293 1 2 1-04
SENSE5
OUT3_4
SENSE4
R294 1 2 1-04
SENSE3
OUT1_2
SENSE2
R273 1 2 1-04
SENSE9
OUT9_10
SENSE10
R258 1 2 1-04
SENSE11
OUT11_12
SENSE12
R247 1 2 1-04

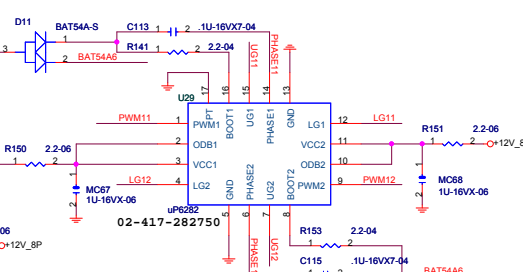
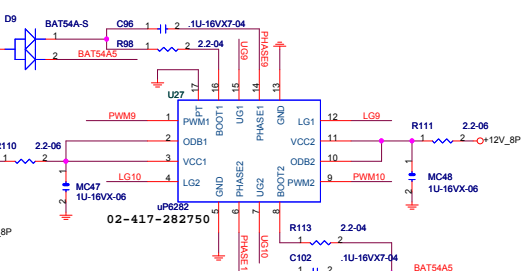
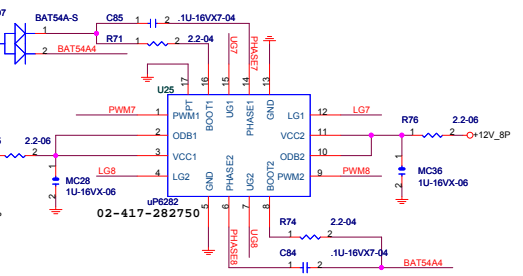
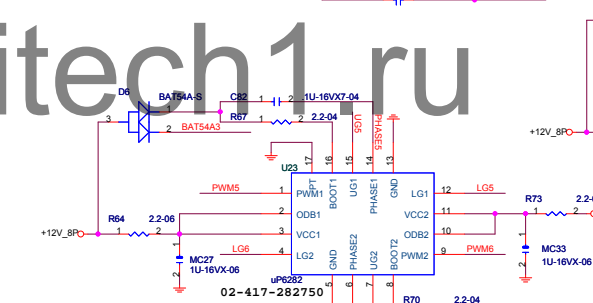
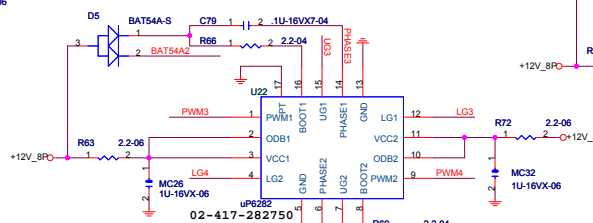
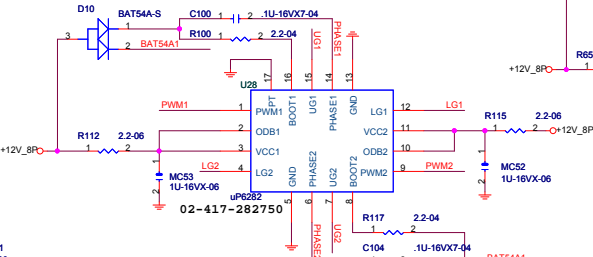
VCC
R227 10K-04
R234 10K-04
VCC3
R243 10K-04
VIN
R239 10K-04
VRM_PWRGD
BC263 010U-04-0
ENPWR
BC305 010U-04-0
R238 1K-04

+12V_8P



UP6225
02-437-225750

OUT7_8 R321 1 2 1-04
OUT8_9 R324 1 2 1-04
OUT3_4 R286 1 2 1-04
OUT1_2 R274 1 2 1-04
OUT9_10 R289 1 2 1-04
OUT11_12 R248 1 2 1-04
IS_7 ER57 1 2 121K-1-04
IS_8 ER56 1 2 121K-1-04
IS_5 ER59 1 2 121K-1-04
IS_6 ER60 1 2 121K-1-04
IS_3 ER63 1 2 121K-1-04
IS_4 ER48 1 2 121K-1-04
IS_1 ER46 1 2 121K-1-04
IS_2 ER44 1 2 121K-1-04
IS_9 ER43 1 2 121K-1-04
IS_10 ER41 1 2 121K-1-04
IS_11 ER39 1 2 121K-1-04
IS_12 ER38 1 2 121K-1-04



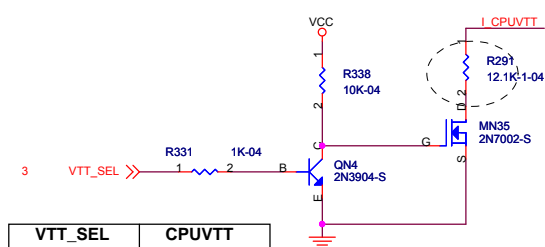
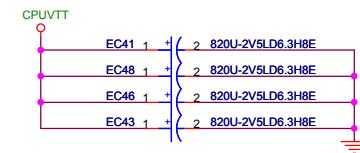
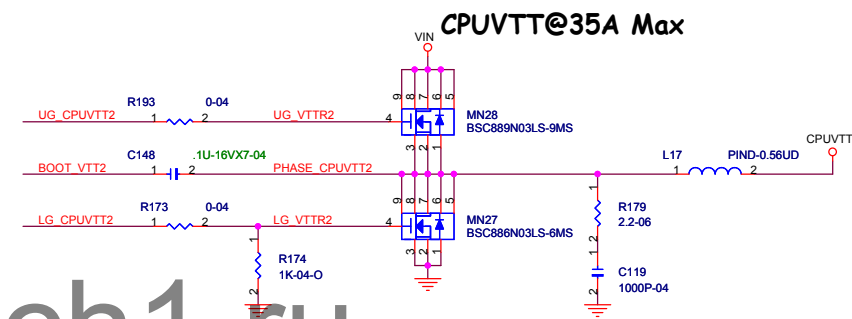
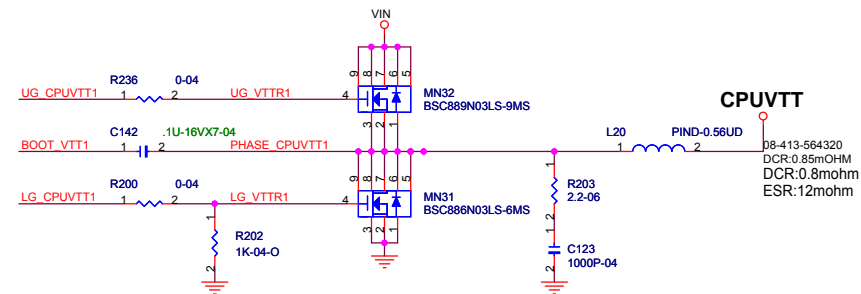
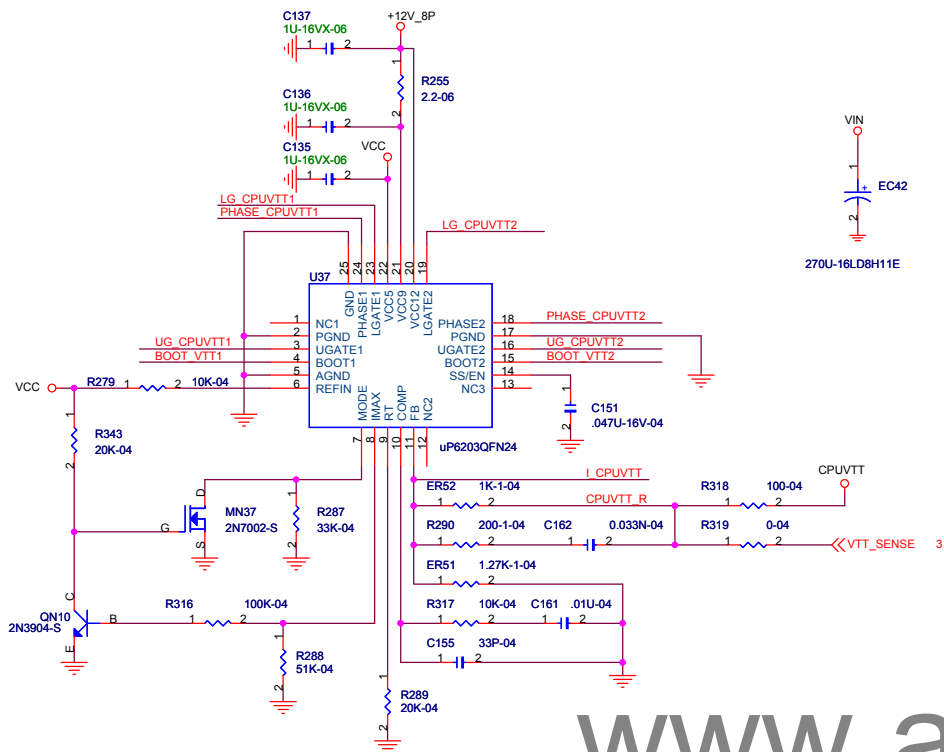
| ADDR | I2C Address | VTT | X | VR11 |
|-------|-------------|-----|-----|-----------|
| VCC/2 | 1000_110x | GND | X | VR10 |
| VCC | 1000_111x | VCC | VTT | AMD 5-BIT |
| GND | 1000_101x | VCC | GND | AMD 6-BIT |

Elitegroup Computer Systems

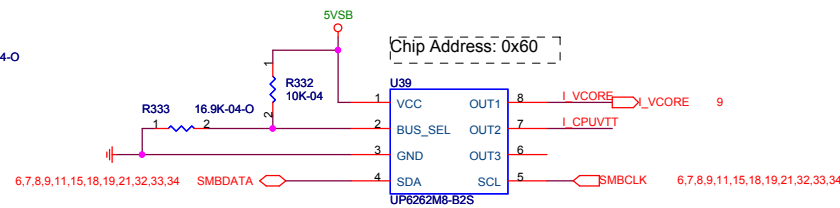
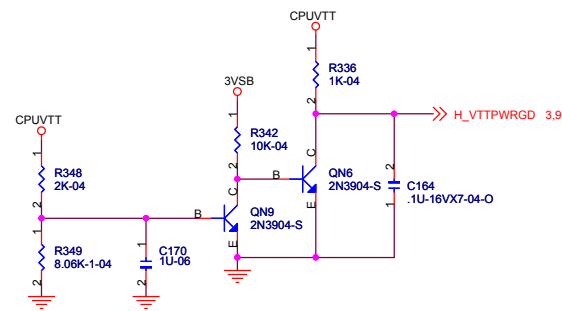
File: CPU VCORE UP6225

Size: Custom Document Number: P55H-AK Rev: 1

Date: Wednesday, June 23, 2010 Sheet: 9 of 35



| VTT_SEL | CPUVTT |
|---------|--------|
| 1 | 1.05V |
| 0 | 1.10V |



uP6262的電流輸出與ΔVout的關係如下：
選取從uP6262輸出的方向為正，則VCORECPUVTT及VAXG的ΔVout為：
ΔVout = -Ic * RFB;
RFB為：
1. For VCORE, RFB = Rvcore = 1K;
2. For CPUVTT, RFB = Rb = 1K;
3. For VAXG, RFB = Rvaxg = 1K.

Solve VTT S3 Leak of Voltage
From Memory Controller.

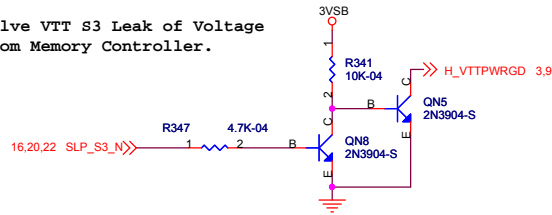
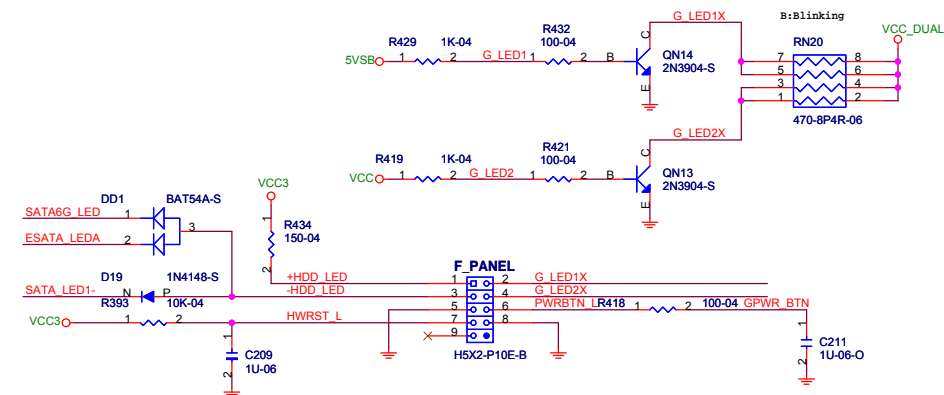
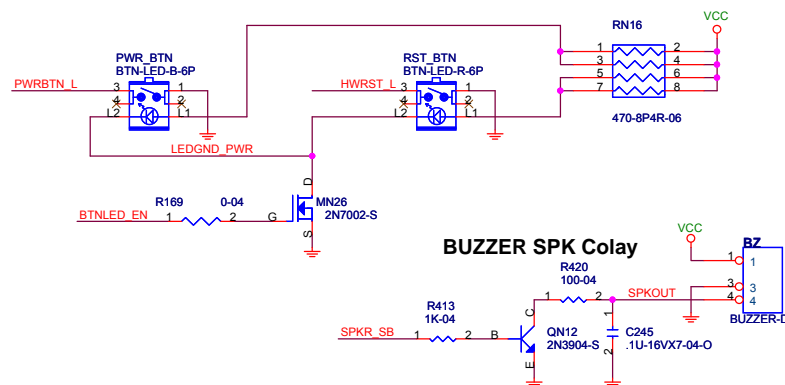


Diagram showing connections for pins 3, 16, 22 and 15, 22:

- Pin 28: SATA6G_LED (to SATA6G_LED)
- Pin 29: ESATA_LED (to ESATA_LED)
- Pin 15: SATA_LED_N (to SATA_LED1-)
- Pin 3, 16: HWRST_N (to HWRST_L)
- Pin 22: G_LED1 (to G_LED1)
- Pin 22: G_LED2 (to G_LED2)
- Pin 16: SPKR (to SPKR_SB)
- Pin 15, 22: BTNLED_EN (to BTNLED_EN)
- Pin 22: GPWR_BTN (to GPWR_BTN)

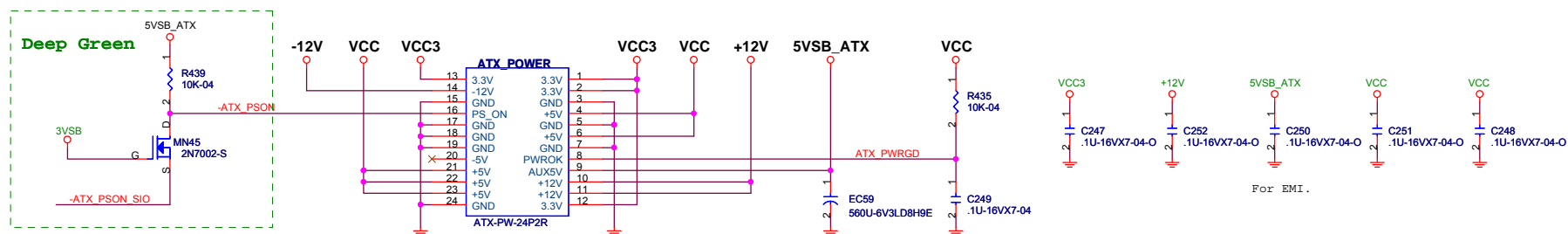


Pin connection diagram for the ATX power supply:

| Left Connector Pin | Right Connector Pin | Signal |
|--------------------|---------------------|--------|
| 1 | 1 | VCC3 |
| 2 | 2 | -12V |
| 3 | 3 | SB5V |
| 4 | 4 | VCC |
| 5 | 5 | +12V |
| 6, 7, 8 | 6, 7 | Ground |

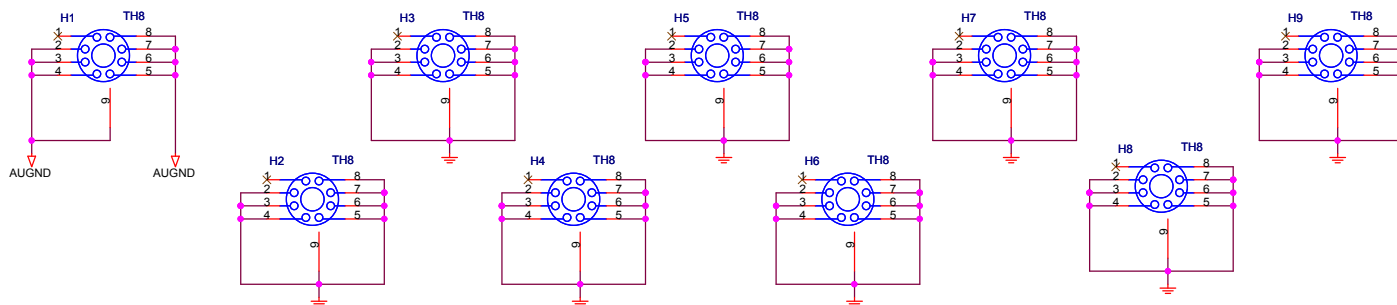
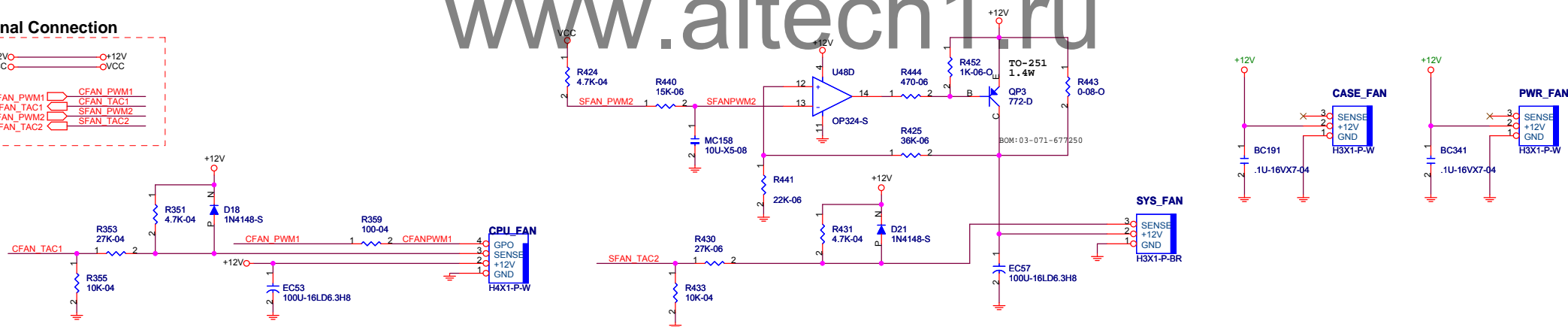
Below the diagram, the ATX power supply pins are labeled:

| Pin | Signal |
|-----|---------------|
| 22 | -ATX_PSON_SIO |
| 22 | ATX_PWRRGD |



Pin 22 connections:

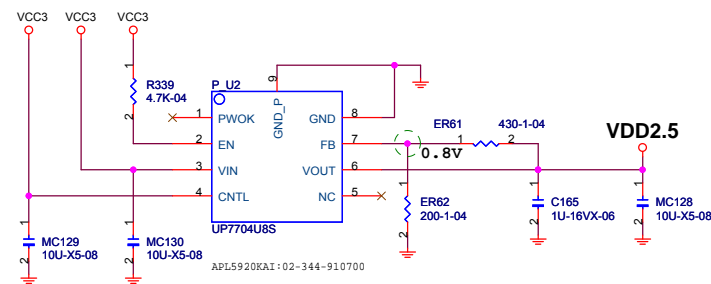
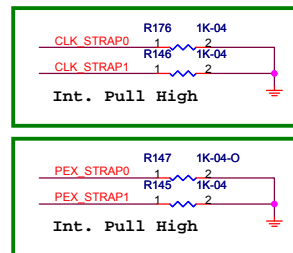
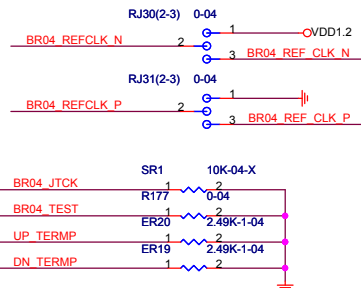
- CFAN_PWM1: +12V
- CFAN_TAC1: VCC
- SFAN_PWM2: +12V
- SFAN_TAC2: VCC



01-201-200992

| | | | | | | | |
|---------------|-------|---|---|---------------|---------------|------|----------------|
| PEG16X_TX_P0 | BC232 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP0 | Y1 | UP0_PEX_RX0_P |
| PEG16X_TX_P1 | BC229 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP1 | AB2 | UP0_PEX_RX1_P |
| PEG16X_TX_P2 | BC226 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP2 | AA3 | UP0_PEX_RX2_P |
| PEG16X_TX_P3 | BC223 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP3 | AB5 | UP0_PEX_RX3_P |
| PEG16X_TX_P4 | BC220 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP4 | AA6 | UP0_PEX_RX4_P |
| PEG16X_TX_P5 | BC217 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP5 | AB8 | UP0_PEX_RX5_P |
| PEG16X_TX_P6 | BC213 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP6 | AA9 | UP0_PEX_RX6_P |
| PEG16X_TX_P7 | BC211 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP7 | AB11 | UP0_PEX_RX7_P |
| PEG16X_TX_P8 | BC208 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP8 | AA13 | UP0_PEX_RX8_P |
| PEG16X_TX_P9 | BC205 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP9 | AB14 | UP0_PEX_RX9_P |
| PEG16X_TX_P10 | BC201 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP10 | AA16 | UP0_PEX_RX10_P |
| PEG16X_TX_P11 | BC197 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP11 | AB17 | UP0_PEX_RX11_P |
| PEG16X_TX_P12 | BC192 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP12 | AA19 | UP0_PEX_RX12_P |
| PEG16X_TX_P13 | BC187 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP13 | AB20 | UP0_PEX_RX13_P |
| PEG16X_TX_P14 | BC181 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP14 | AA22 | UP0_PEX_RX14_P |
| PEG16X_TX_P15 | BC176 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXP15 | Y21 | UP0_PEX_RX15_P |
| PEG16X_TX_N0 | BC230 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN0 | AA1 | UP0_PEX_RX0_N |
| PEG16X_TX_N1 | BC227 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN1 | AB3 | UP0_PEX_RX1_N |
| PEG16X_TX_N2 | BC224 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN2 | AA4 | UP0_PEX_RX2_N |
| PEG16X_TX_N3 | BC221 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN3 | AB6 | UP0_PEX_RX3_N |
| PEG16X_TX_N4 | BC219 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN4 | AA7 | UP0_PEX_RX4_N |
| PEG16X_TX_N5 | BC215 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN5 | AB9 | UP0_PEX_RX5_N |
| PEG16X_TX_N6 | BC212 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN6 | AA10 | UP0_PEX_RX6_N |
| PEG16X_TX_N7 | BC209 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN7 | AB12 | UP0_PEX_RX7_N |
| PEG16X_TX_N8 | BC206 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN8 | AA14 | UP0_PEX_RX8_N |
| PEG16X_TX_N9 | BC202 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN9 | AB15 | UP0_PEX_RX9_N |
| PEG16X_TX_N10 | BC199 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN10 | AA17 | UP0_PEX_RX10_N |
| PEG16X_TX_N11 | BC195 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN11 | AB18 | UP0_PEX_RX11_N |
| PEG16X_TX_N12 | BC188 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN12 | AA20 | UP0_PEX_RX12_N |
| PEG16X_TX_N13 | BC183 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN13 | AB21 | UP0_PEX_RX13_N |
| PEG16X_TX_N14 | BC178 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN14 | Y22 | UP0_PEX_RX14_N |
| PEG16X_TX_N15 | BC171 | 1 | 2 | 1U-16VX7-04 | BR04 PE RXN15 | W21 | UP0_PEX_RX15_N |
| PEG16X_RX_P0 | SC60 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP0 | Y3 | UP0_PEX_TX0_P |
| PEG16X_RX_P1 | SC58 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP1 | W5 | UP0_PEX_TX1_P |
| PEG16X_RX_P2 | SC55 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP2 | V7 | UP0_PEX_TX2_P |
| PEG16X_RX_P3 | SC57 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP3 | Y8 | UP0_PEX_TX3_P |
| PEG16X_RX_P4 | SC52 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP4 | Y9 | UP0_PEX_TX4_P |
| PEG16X_RX_P5 | SC47 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP5 | W9 | UP0_PEX_TX5_P |
| PEG16X_RX_P6 | SC40 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP6 | Y11 | UP0_PEX_TX6_P |
| PEG16X_RX_P7 | SC35 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP7 | W12 | UP0_PEX_TX7_P |
| PEG16X_RX_P8 | SC39 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP8 | Y14 | UP0_PEX_TX8_P |
| PEG16X_RX_P9 | SC25 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP9 | W15 | UP0_PEX_TX9_P |
| PEG16X_RX_P10 | SC18 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP10 | Y17 | UP0_PEX_TX10_P |
| PEG16X_RX_P11 | SC19 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP11 | W16 | UP0_PEX_TX11_P |
| PEG16X_RX_P12 | SC16 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP12 | Y18 | UP0_PEX_TX12_P |
| PEG16X_RX_P13 | SC12 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP13 | W19 | UP0_PEX_TX13_P |
| PEG16X_RX_P14 | SC10 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP14 | Y19 | UP0_PEX_TX14_P |
| PEG16X_RX_P15 | SC14 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXP15 | T18 | UP0_PEX_TX15_P |
| PEG16X_RX_N0 | SC61 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN0 | W4 | UP0_PEX_TX0_N |
| PEG16X_RX_N1 | SC59 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN1 | Y5 | UP0_PEX_TX1_N |
| PEG16X_RX_N2 | SC54 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN2 | W7 | UP0_PEX_TX2_N |
| PEG16X_RX_N3 | SC56 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN3 | Y8 | UP0_PEX_TX3_N |
| PEG16X_RX_N4 | SC53 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN4 | W9 | UP0_PEX_TX4_N |
| PEG16X_RX_N5 | SC48 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN5 | Y9 | UP0_PEX_TX5_N |
| PEG16X_RX_N6 | SC46 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN6 | W11 | UP0_PEX_TX6_N |
| PEG16X_RX_N7 | SC39 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN7 | Y12 | UP0_PEX_TX7_N |
| PEG16X_RX_N8 | SC33 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN8 | W14 | UP0_PEX_TX8_N |
| PEG16X_RX_N9 | SC28 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN9 | Y15 | UP0_PEX_TX9_N |
| PEG16X_RX_N10 | SC17 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN10 | W17 | UP0_PEX_TX10_N |
| PEG16X_RX_N11 | SC24 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN11 | Y16 | UP0_PEX_TX11_N |
| PEG16X_RX_N12 | SC15 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN12 | W18 | UP0_PEX_TX12_N |
| PEG16X_RX_N13 | SC11 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN13 | Y20 | UP0_PEX_TX13_N |
| PEG16X_RX_N14 | SC9 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN14 | W20 | UP0_PEX_TX14_N |
| PEG16X_RX_N15 | SC13 | 1 | 2 | 1U-16VX7-04-X | BR04 PE TXN15 | T19 | UP0_PEX_TX15_N |

NF200-SLI-A3



Elitegroup Computer Systems

Title: **DUAL PCIE CTRL NV NF200**

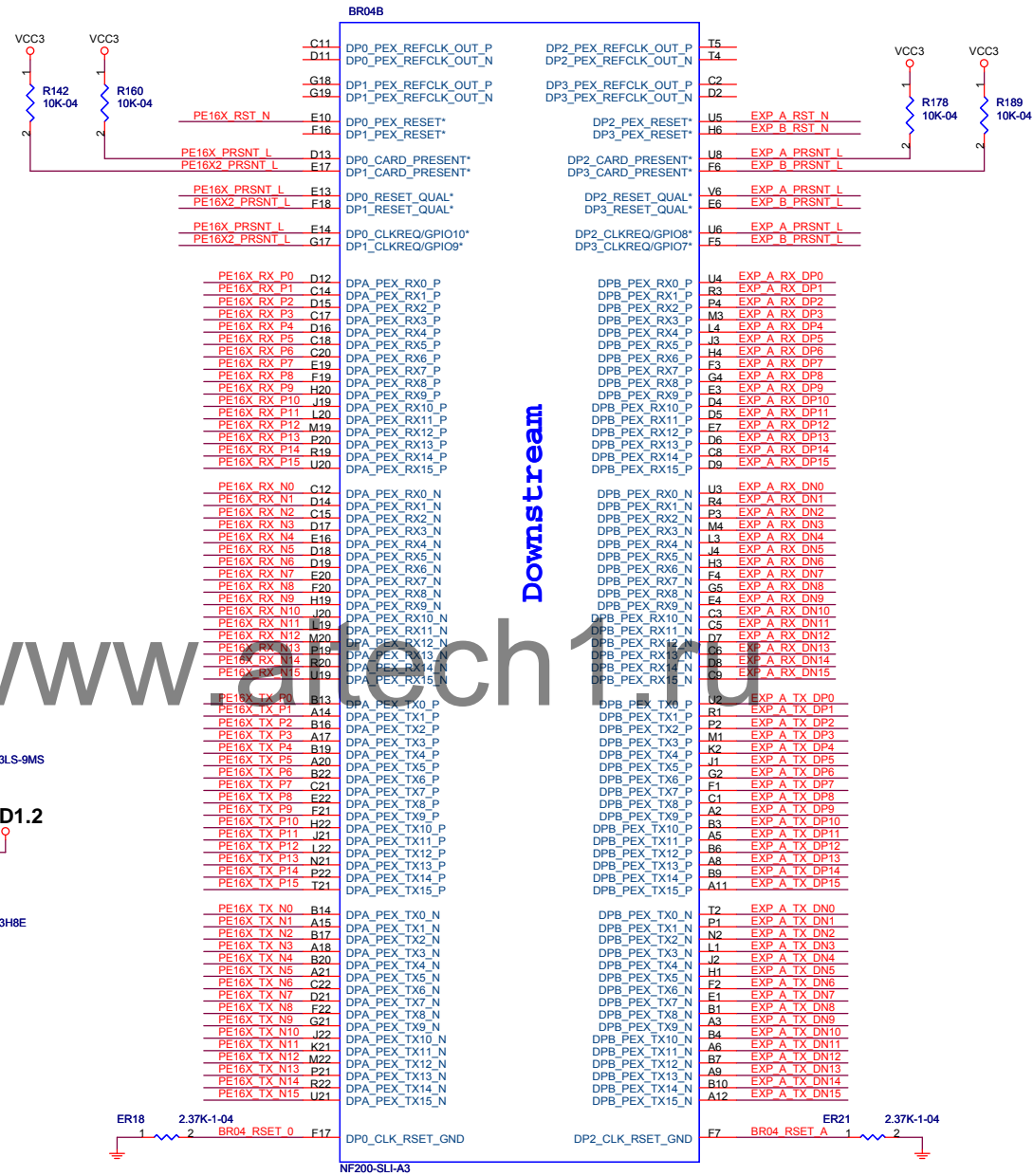
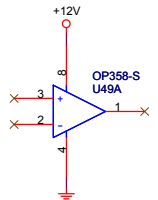
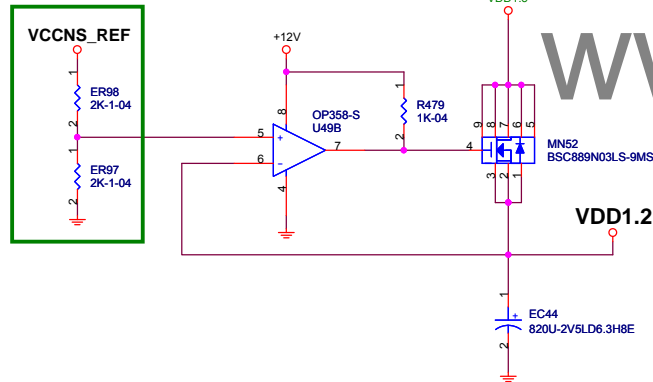
Size: Document Number: **P55H-AK** Rev: 1

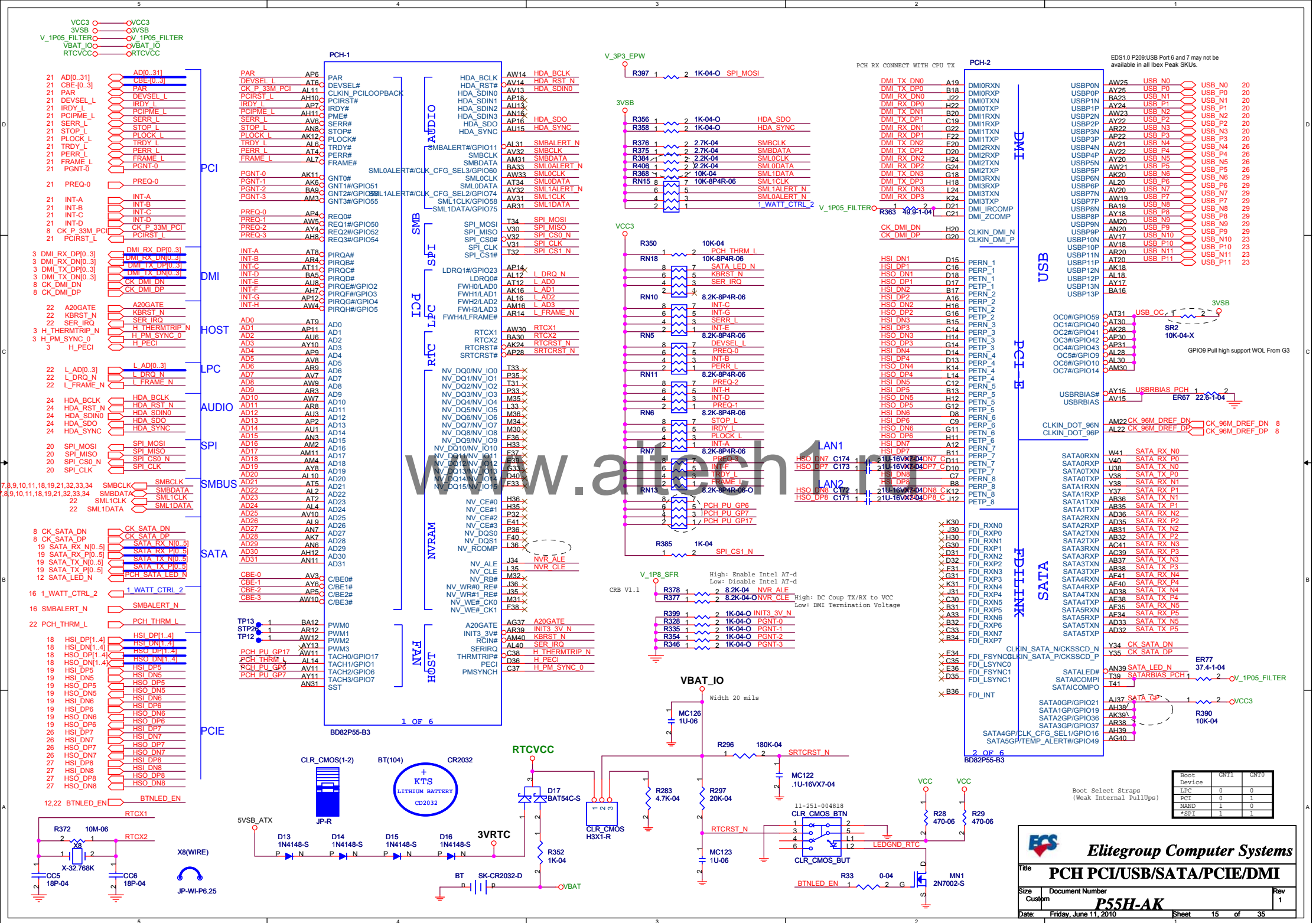
Date: Friday, June 11, 2010 Sheet: 13 of 35

32 PE16X_RX_P[0:15] PE16X_RX_P[15:0]
32 PE16X_RX_N[0:15] PE16X_RX_N[15:0]
32 PE16X_TX_P[15:0] PE16X_TX_P[15:0]
32 PE16X_TX_N[15:0] PE16X_TX_N[15:0]
32 PE16X_RST_N PE16X_RST_N
32 PE16X_PRSENT_L PE16X_PRSENT_L

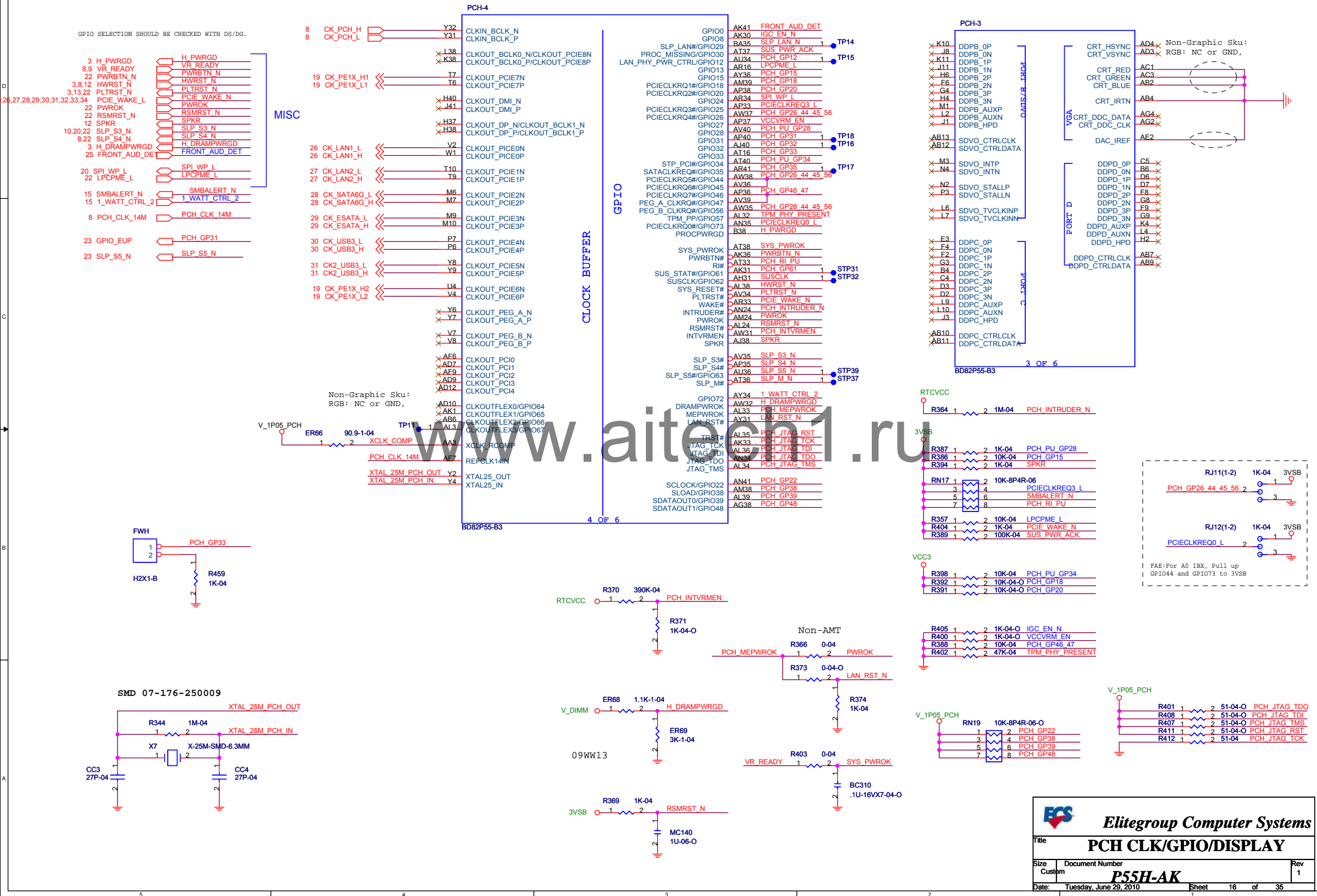
33 EXP_A_RX_DP[0..7] EXP_A_RX_DP[0..7]
33 EXP_A_RX_DN[0..7] EXP_A_RX_DN[0..7]
33 EXP_A_TX_DP[0..7] EXP_A_TX_DP[0..7]
33 EXP_A_TX_DN[0..7] EXP_A_TX_DN[0..7]
33 EXP_A_RST_N EXP_A_RST_N
33 EXP_A_PRSENT_L EXP_A_PRSENT_L

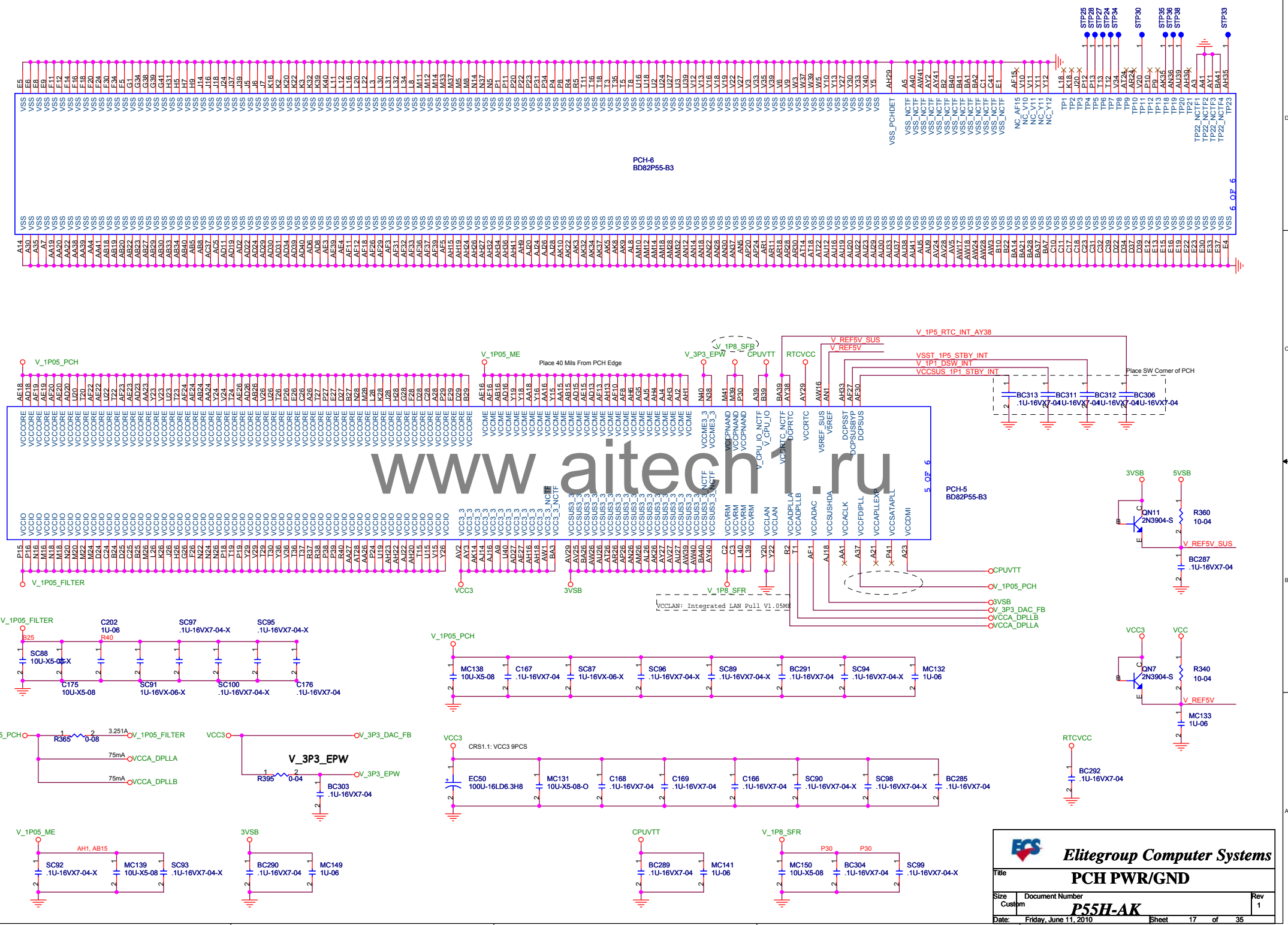
34 EXP_A_RX_DP[8..15] EXP_A_RX_DP[8..15]
34 EXP_A_RX_DN[8..15] EXP_A_RX_DN[8..15]
34 EXP_A_TX_DP[8..15] EXP_A_TX_DP[8..15]
34 EXP_A_TX_DN[8..15] EXP_A_TX_DN[8..15]
34 EXP_B_RST_N EXP_B_RST_N
34 EXP_B_PRSENT_L EXP_B_PRSENT_L

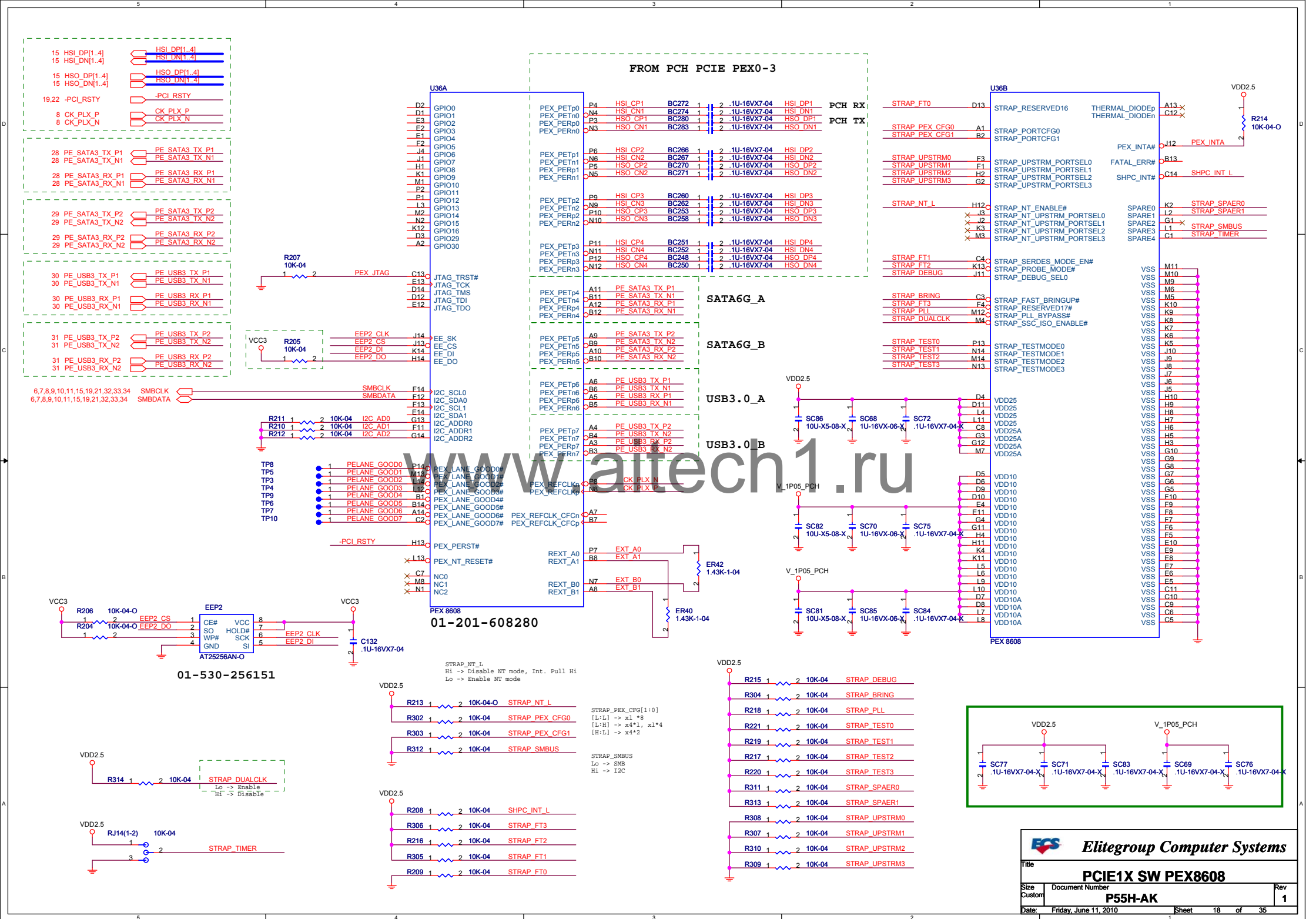




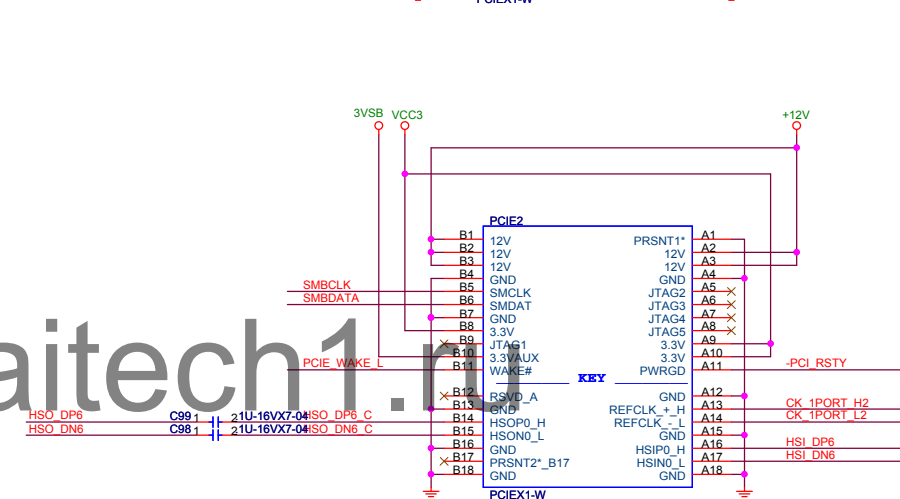
GPIO SELECTION SHOULD BE CHECKED WITH DS/DG.







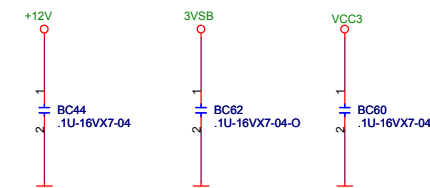
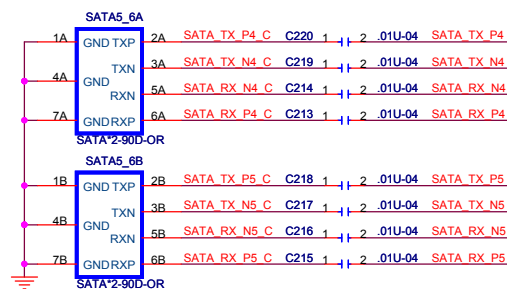
| | | | |
|---------------------------------|-------------|---------------------------------|-------------|
| 16 | CK_PE1X_H1 | 16 | CK_1PORT_H1 |
| 16 | CK_PE1X_L1 | 16 | CK_1PORT_L1 |
| 15 | HSL_DP5 | 15 | HSI_DP5 |
| 15 | HSL_DN5 | 15 | HSI_DN5 |
| 15 | HSO_DP5 | 15 | HSO_DP5 |
| 15 | HSO_DN5 | 15 | HSO_DN5 |
| 16 | CK_PE1X_H2 | 16 | CK_1PORT_H2 |
| 16 | CK_PE1X_L2 | 16 | CK_1PORT_L2 |
| 15 | HSL_DP6 | 15 | HSI_DP6 |
| 15 | HSL_DN6 | 15 | HSI_DN6 |
| 15 | HSO_DP6 | 15 | HSO_DP6 |
| 15 | HSO_DN6 | 15 | HSO_DN6 |
| 18,22 | -PCI_RSTY | 18,22 | -PCI_RSTY |
| 26,27,28,29,30,31,32,33,34 | PCIE_WAKE_L | 26,27,28,29,30,31,32,33,34 | PCIE_WAKE_L |
| 6,7,8,9,10,11,15,18,21,32,33,34 | SMBCLK | 6,7,8,9,10,11,15,18,21,32,33,34 | SMBCLK |
| 7,8,9,10,11,15,18,21,32,33,34 | SMBDATA | 7,8,9,10,11,15,18,21,32,33,34 | SMBDATA |



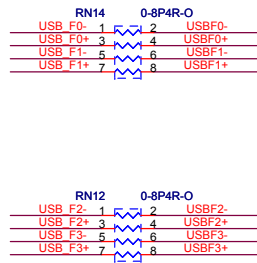
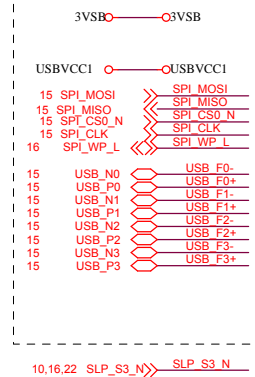
The diagram shows four signal traces over time:

- SATA_RX_N[0..5]**: A blue signal trace with a red arrow pointing to its start.
- SATA_RX_P[0..5]**: A blue signal trace with a red arrow pointing to its start.
- SATA_TX_N[0..5]**: A blue signal trace with a red arrow pointing to its start.
- SATA_TX_P[0..5]**: A blue signal trace with a red arrow pointing to its start.

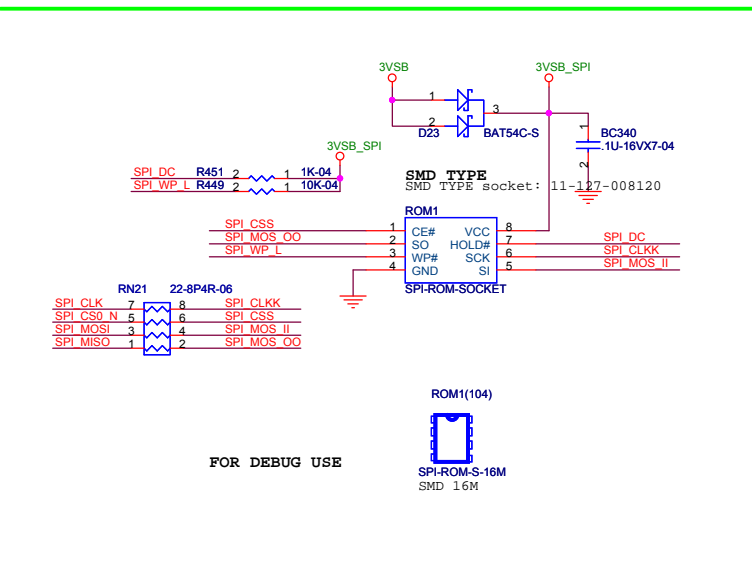
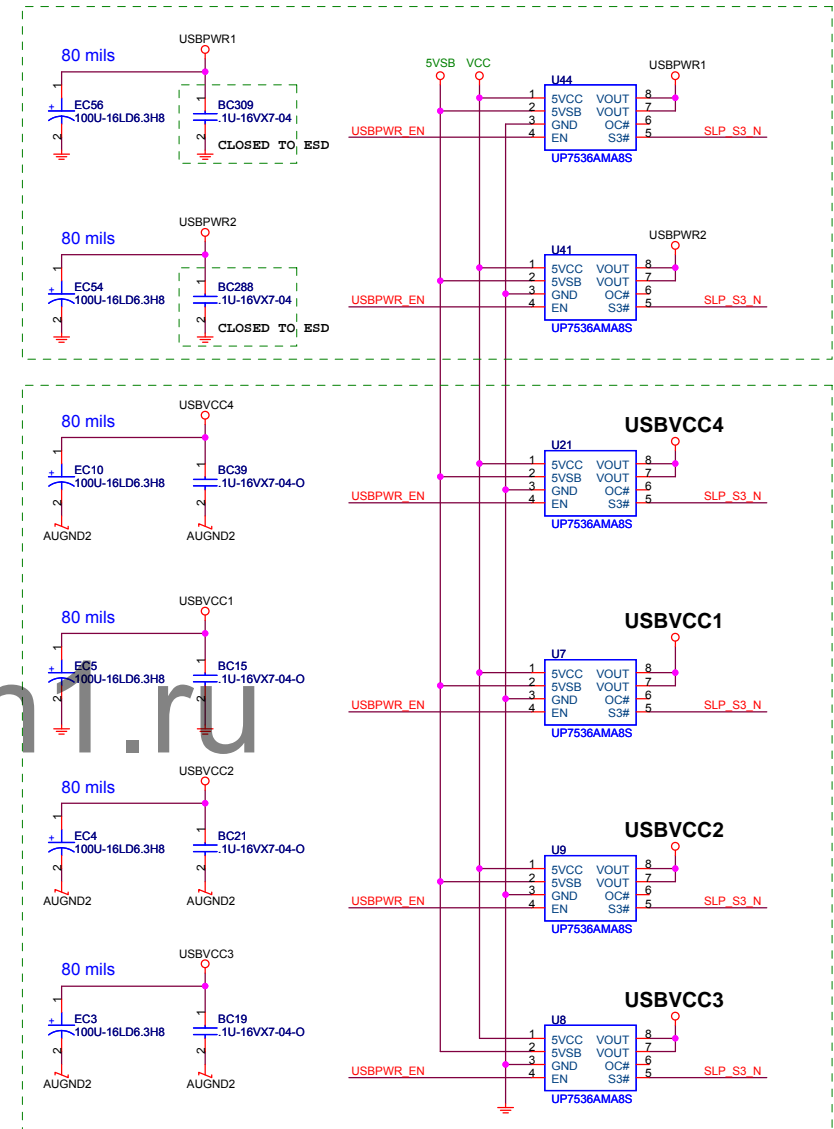
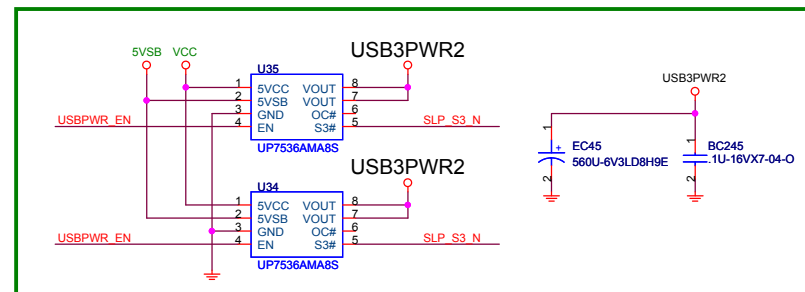
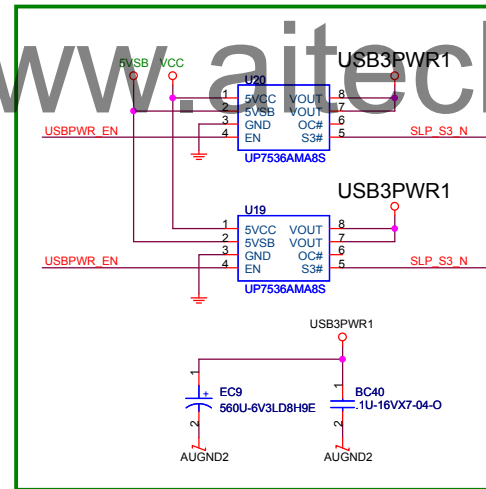
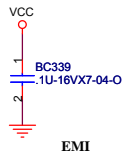
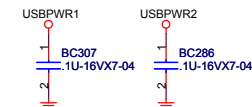
The signals are grouped into two pairs, each with a red bracket on the left. The first pair (RX) is labeled with a red '1' and the second pair (TX) is labeled with a red '2'.



External Connection



FRONT_SIDE



| | |
|-------------|-----------------------|
| TitleBlock3 | |
| Title | USB/SPI/Rear IO |
| Size | Document Number |
| Custom | P55H-AK |
| Date: | Friday, June 18, 2010 |
| Sheet | 20 of 35 |
| Rev | 1 |

VCC
VCC3
3VSB
+12V
-12V

External Connection

SMBCLK
SMBDATA
PCIRST_L

COMMON

AD[0..31]
CBE[0..3]

PAR
PERR_L
PLOCK_L
STOP_L
DEVSEL_L
TRDY_L
IRDY_L
FRAME_L
SERR_L
PCIPME_L

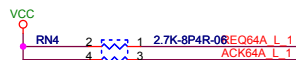
AD[0..31]
CBE[0..3]

PAR
PERR_L
PLOCK_L
STOP_L
DEVSEL_L
TRDY_L
IRDY_L
FRAME_L
SERR_L
PCIPME_L

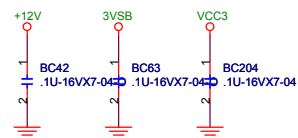
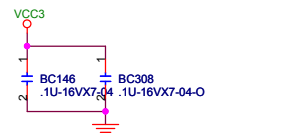
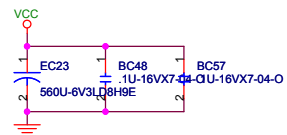
PGNT-0
PREQ-0

INT-A
INT-B
INT-C
INT-D

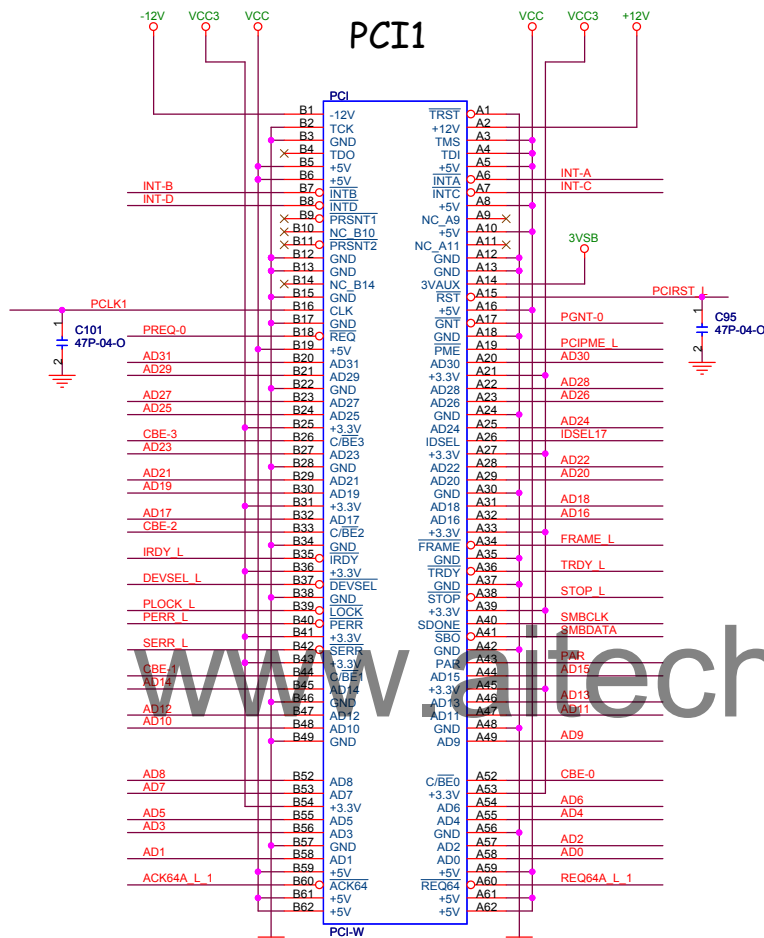
PCLK1



AD17 R120 1 300-04 IDSEL17

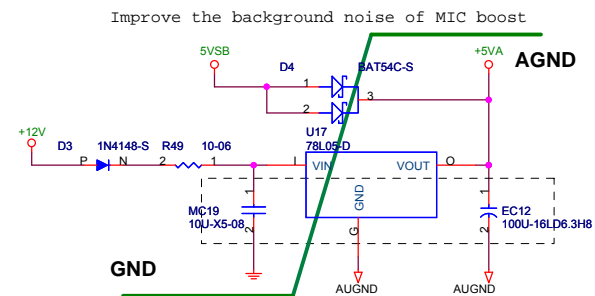
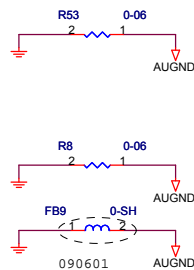
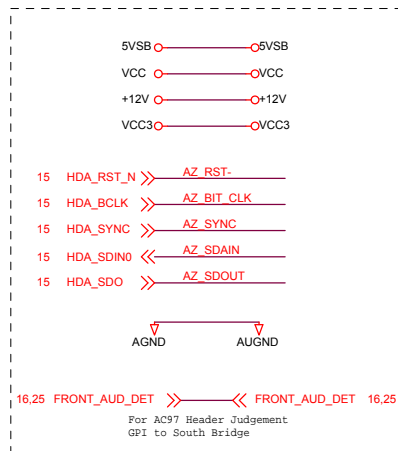


PCI1

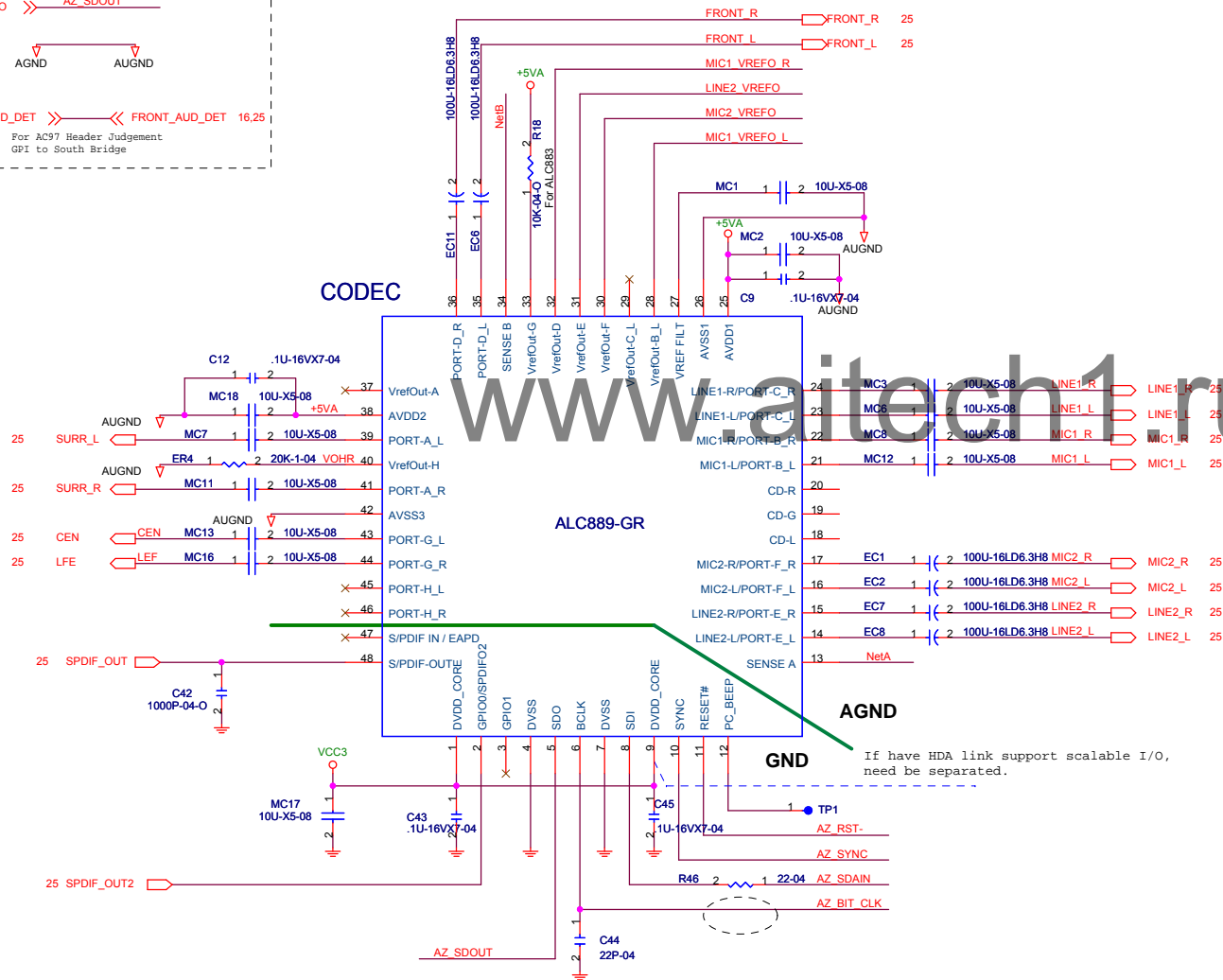


PCI-INT: IDSEL=AD17
INTA: INTA REQ=PREQ0#
INTB: INTB GNT=PGNT0#
INTC: INTC
INTD: INTD

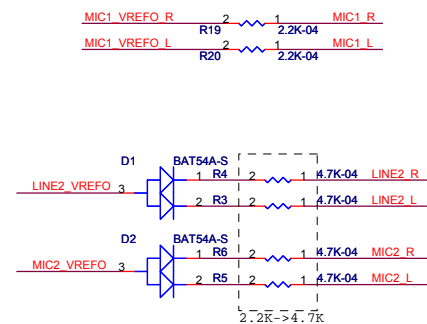
External Connection



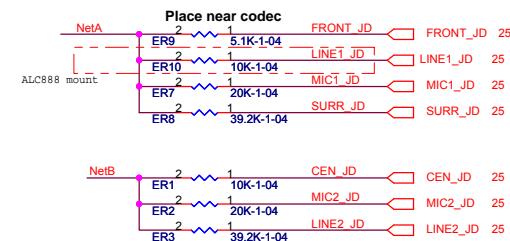
CODEC



Verfourt bias for stereo microphone.

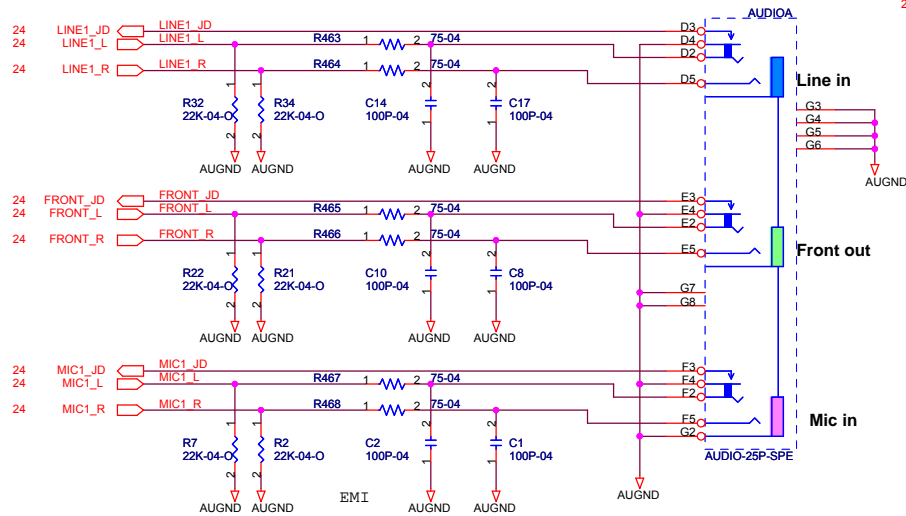


Resistors Networks

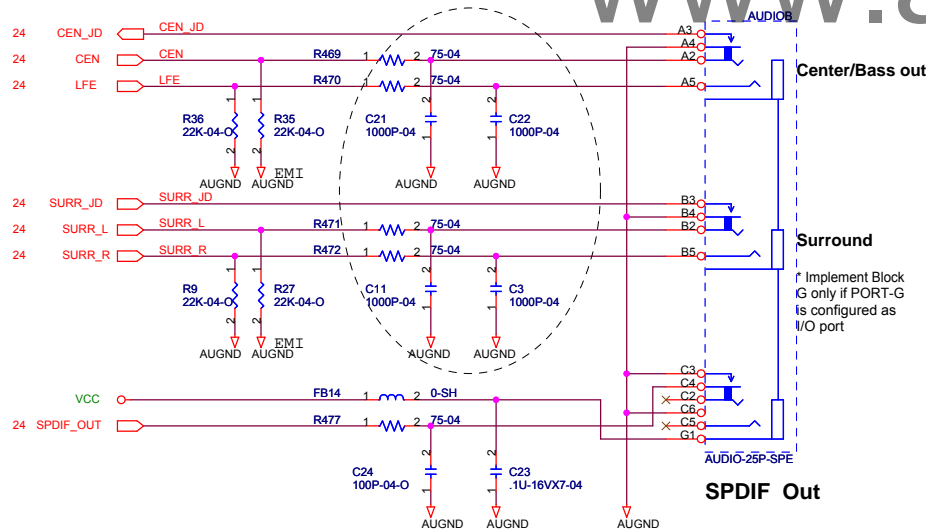


08.05.08 follow Realtek's suggestion

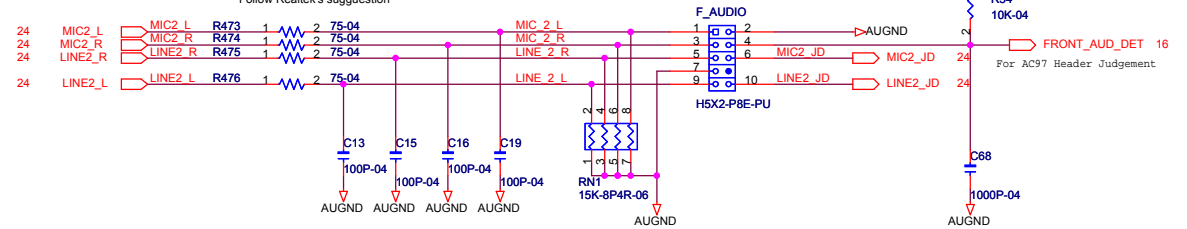
Rear Panel Onboard Analog I/O



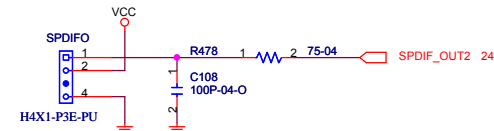
Rear Panel (Optional Rear Audio Panel)



Follow Realtek's suggestion

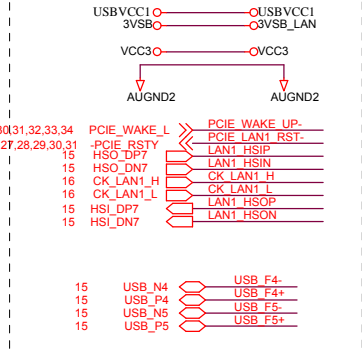


SPDIF-OUT



www.aitech1.ru

External Connection



When you found some bug, please inform Ren(ext:26150) to update circuit.

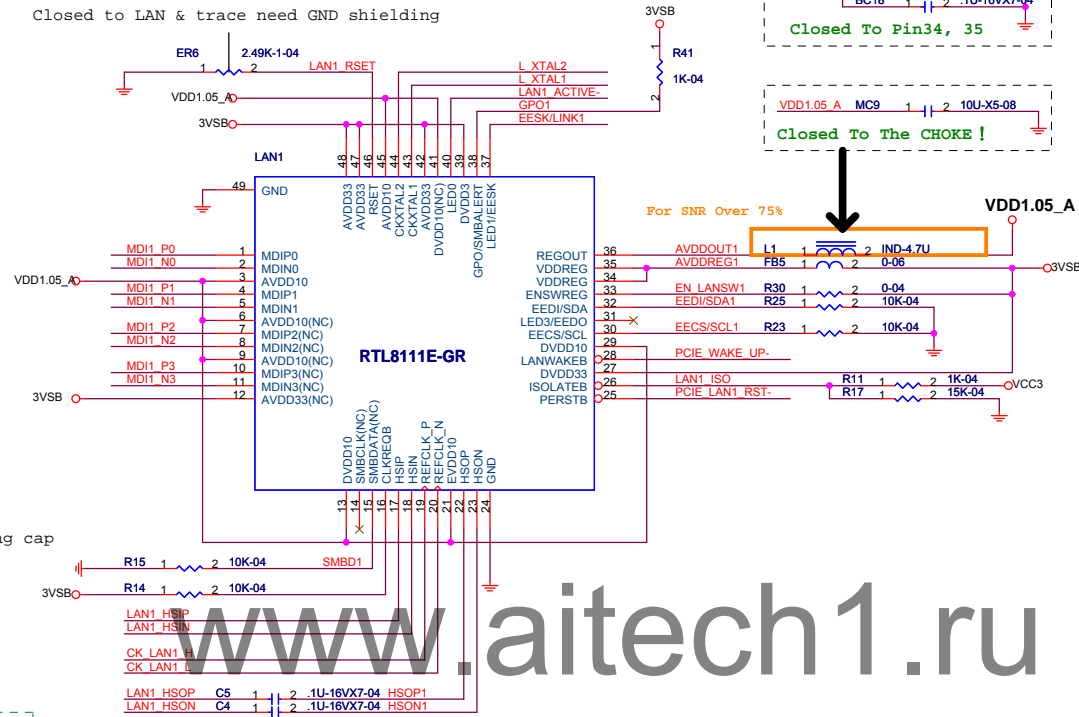
新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

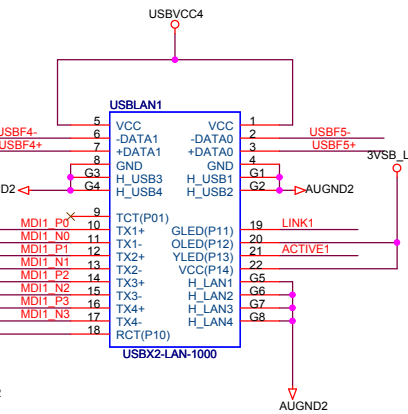
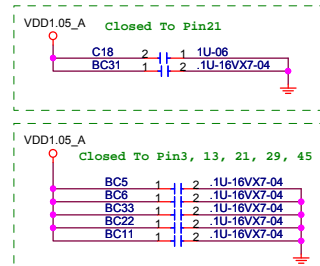
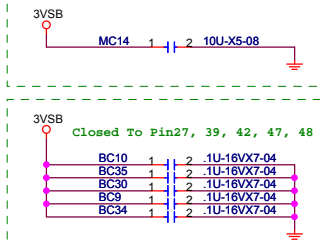
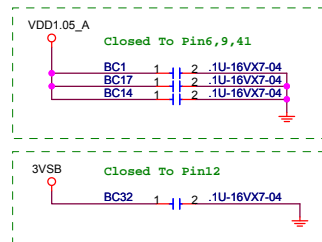
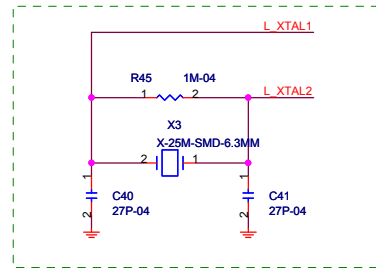
LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

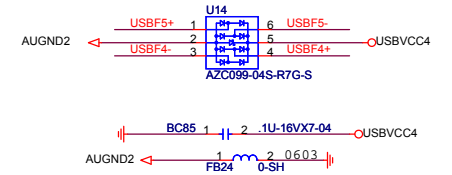
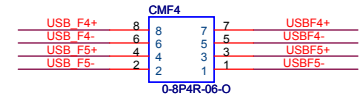
Closed to LAN & trace need GND shielding

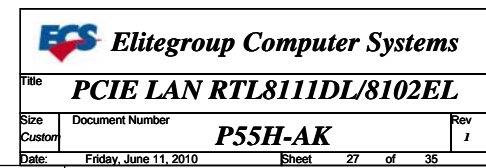


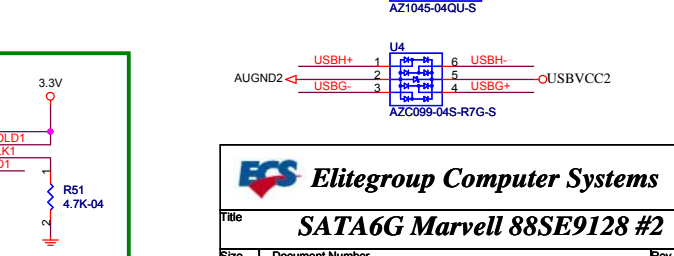
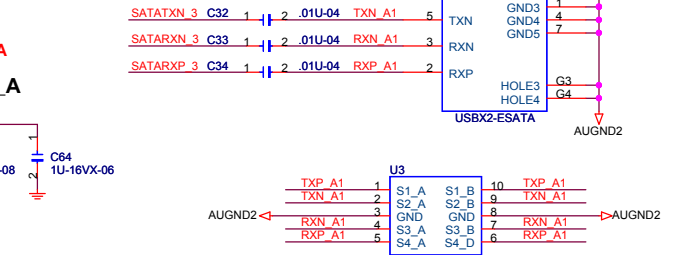
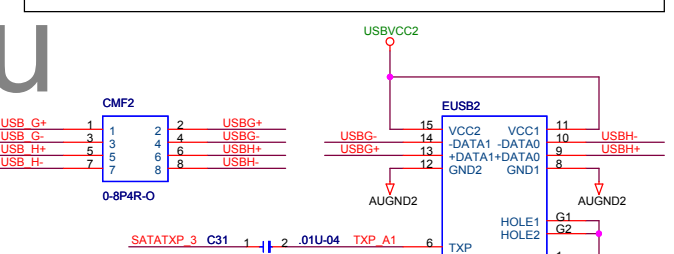
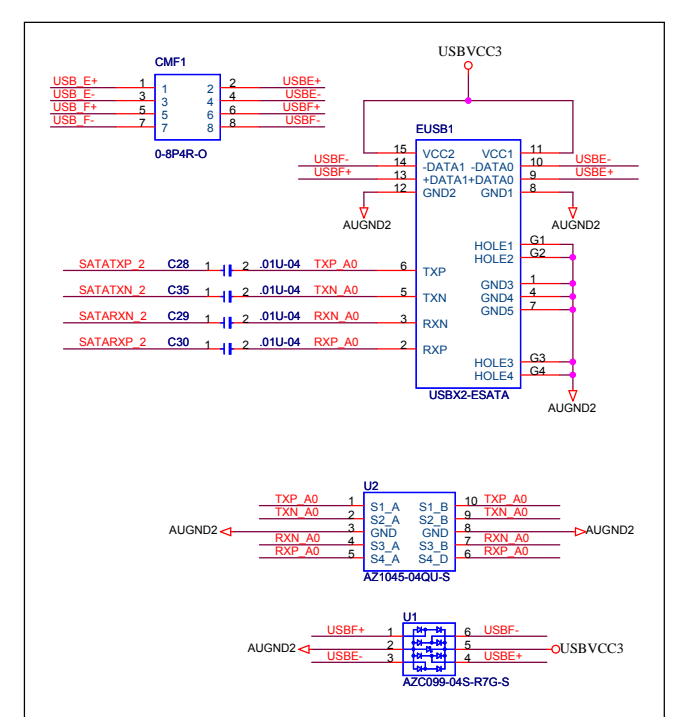
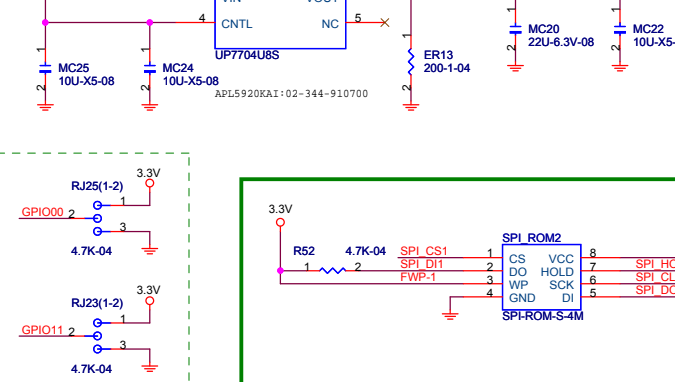
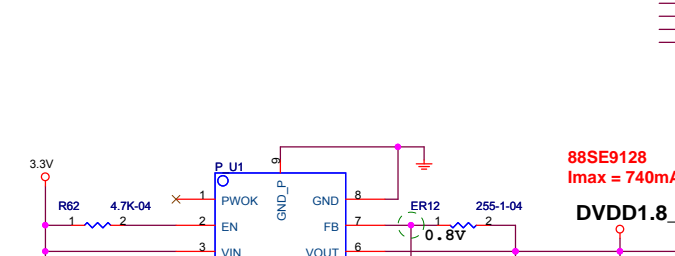
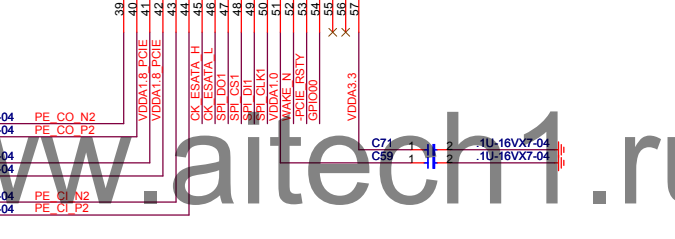
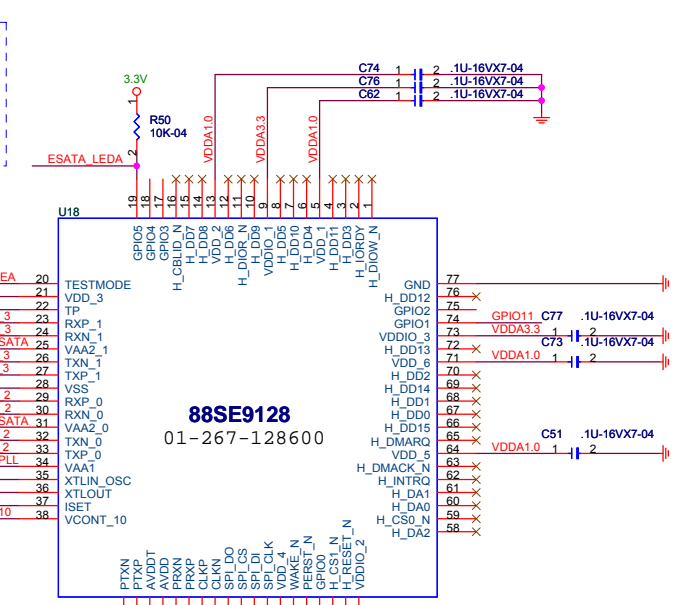
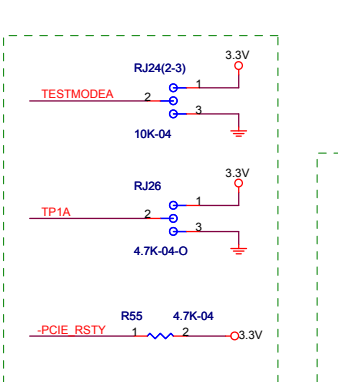
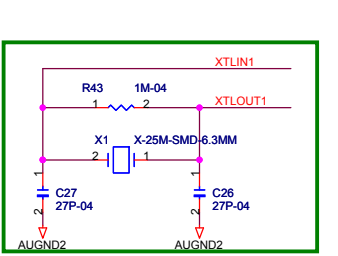
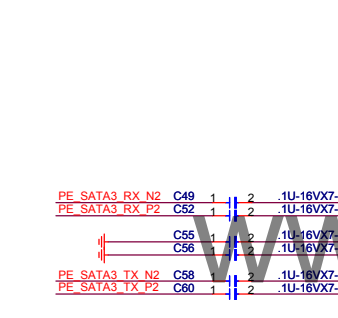
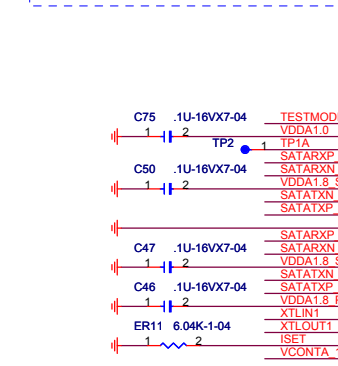
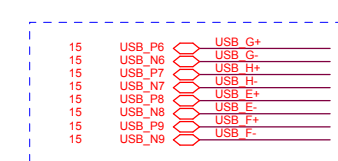
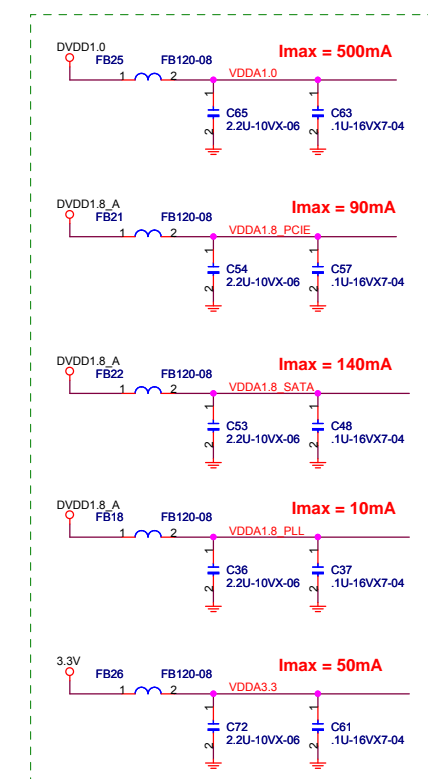
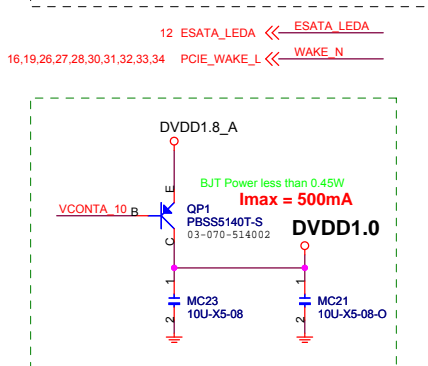
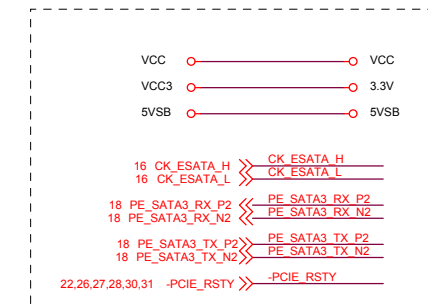
www.aitech1.ru



Link: Green on
Active: Yellow blinking

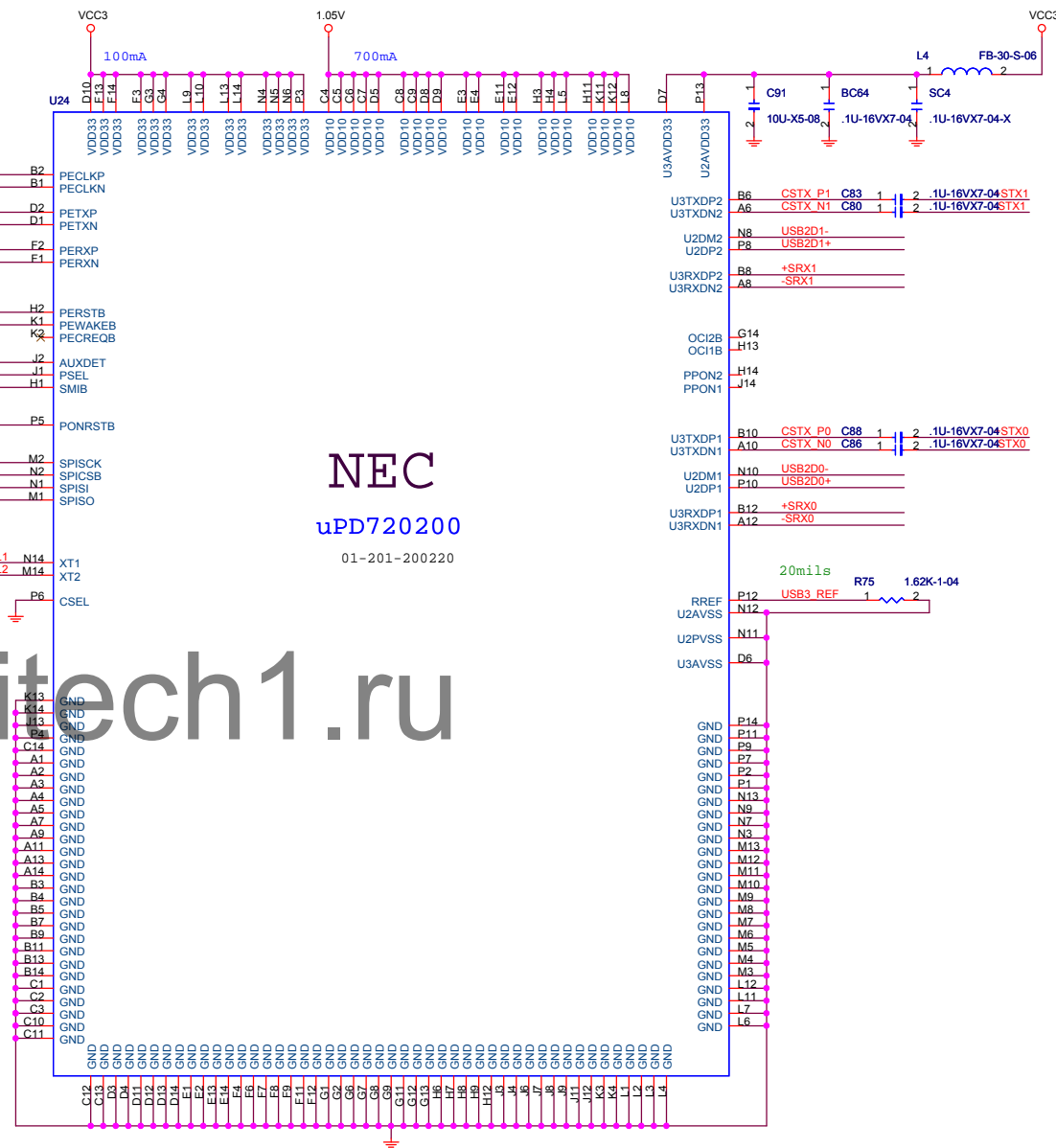
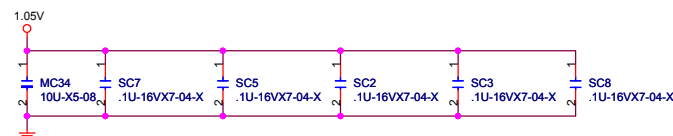
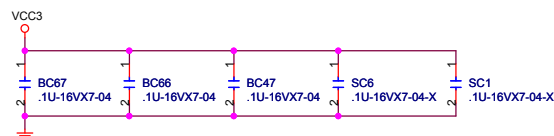
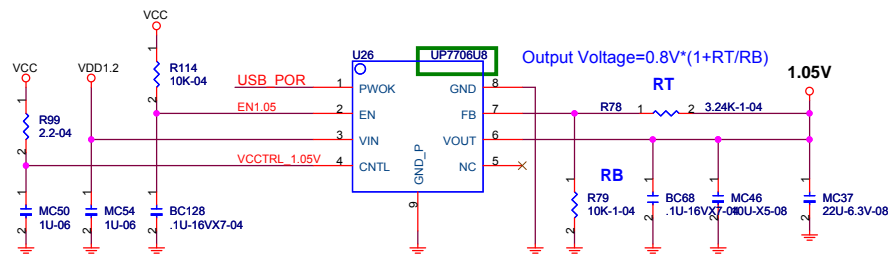
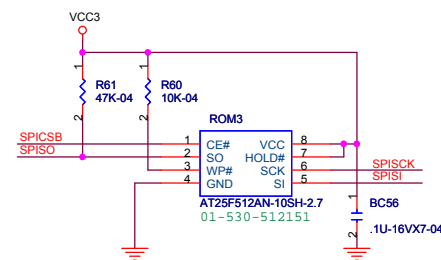
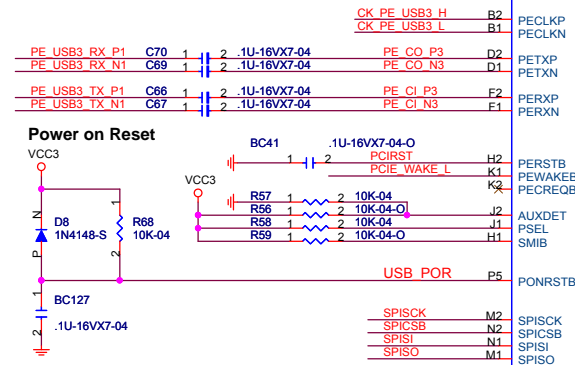
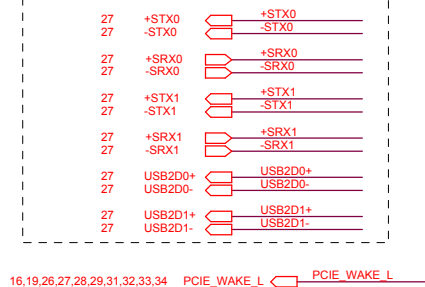






22,26,27,28,29,31 - PCIE_RSTY  PCIRST

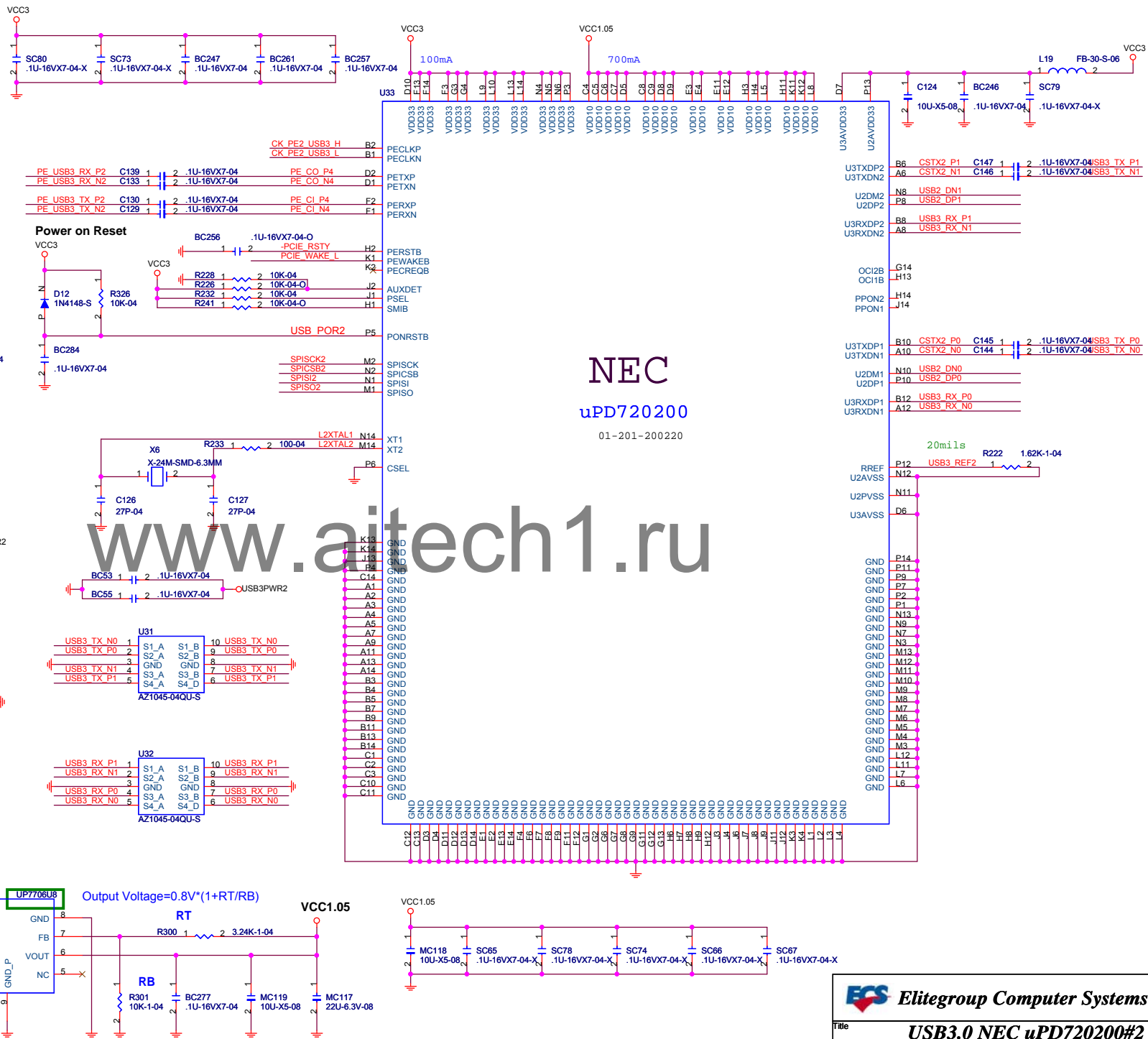
| | | |
|------------------|---|---------------|
| 18 PE_USB3_TX_P1 |  | PE_USB3_TX P1 |
| 18 PE_USB3_TX_N1 |  | PE_USB3_TX N1 |
| 18 PE_USB3_RX_P1 |  | PE_USB3_RX P1 |
| 18 PE_USB3_RX_N1 |  | PE_USB3_RX N1 |
| 16 CK_USB3_H |  | CK PE_USB3_H |
| 16 CK_USB3_L |  | CK PE_USB3_L |

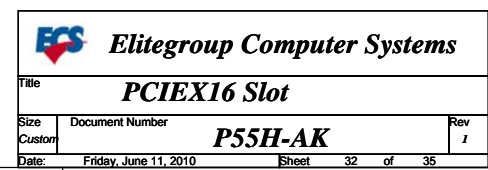
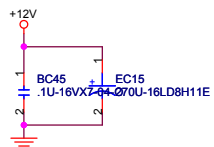
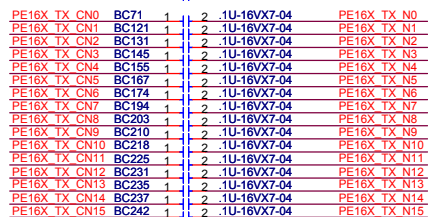


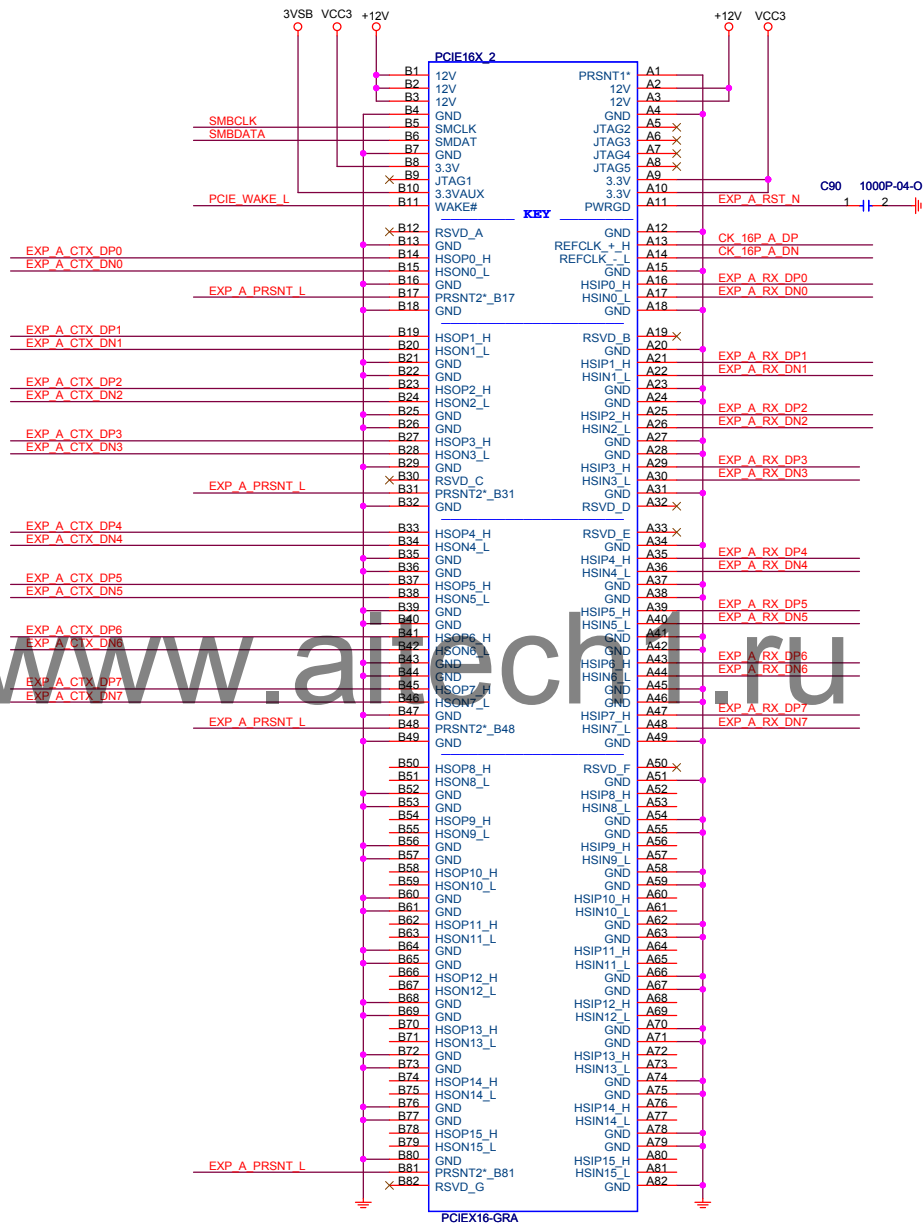
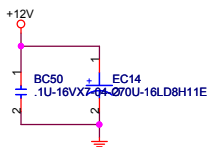
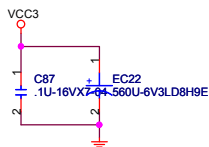
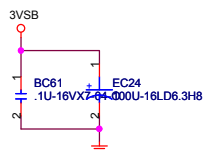
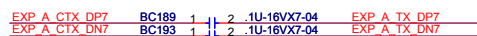
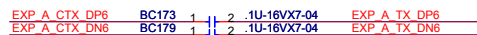
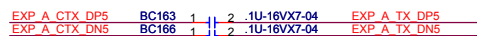
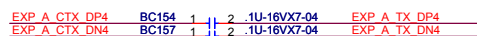
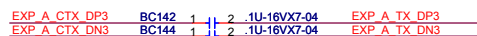
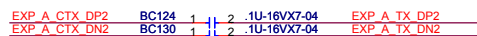
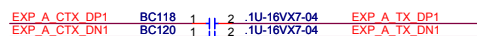
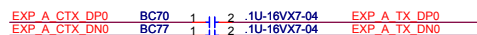
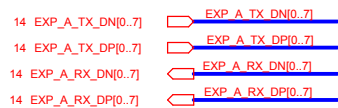
NEC
uPD720200

01-201-200220

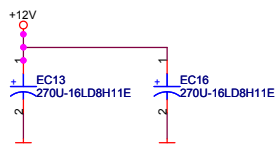
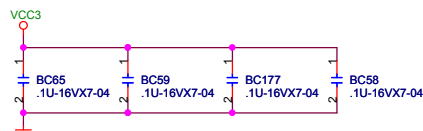
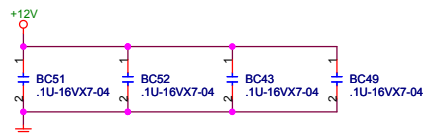
07-135-240024 -> DIP
07-176-240009 -> SMD
crystal 2p 6x3 5mm smd





PCIEX8_A

| | | | |
|----|--------------------|---|--------------------|
| 14 | EXP_A_TX_DN[8..15] |  | EXP_A_TX_DN[8..15] |
| 14 | EXP_A_TX_DP[8..15] |  | EXP_A_TX_DP[8..15] |
| 14 | EXP_A_RX_DN[8..15] |  | B EXP_A_RX_DN[0:7] |
| 14 | EXP_A_RX_DP[8..15] |  | B EXP_A_RX_DP[0:7] |
| 8 | CK_16P_B_DP |  | CK_16P_B_DP |
| 8 | CK_16P_B_DN |  | CK_16P_B_DN |
| 14 | EXP_B_PRNST_L |  | EXP_B_PRNST_L |
| 14 | EXP_B_RST_N |  | EXP_B_RST_N |



9 UG[1:12] >> UG[1:12]
 9 PHASE[1:12] >> PHASE[1:12]
 9 LG[1:12] >> LG[1:12]
 9 IS_1[1:12] << IS_1[1:12]
 9 SENSE[1:12] << SENSE[1:12]
 9 OUT1_2 << OUT1_2
 9 OUT3_4 << OUT3_4
 9 OUT5_6 << OUT5_6
 9 OUT7_8 << OUT7_8
 9 OUT9_10 << OUT9_10
 9 OUT11_12 << OUT11_12

